72-1002-C

Instruction Manual

for

MODEL 5740
MULTIFUNCTION COUNTER

DATA PRECISION

72-1002-C

Instruction Manual

for

MODEL 5740
MULTIFUNCTION COUNTER

Specifications
Operation
Theory of Operation
Maintenance
Parts Lists
Schematics

DATA PRECISION

COPYRIGHT 1975

DATA PRECISION CORPORATION

PRINTED IN U.S.A.

Second Edition - March 1977

PROPRIETARY NOTICE

The information contained in this publication is derived in part from proprietary and patent data of the Data Precision Corporation. This information has been prepared for the express purpose of assisting operating and maintenance personnel in the efficient use of the Model 5740 Multifunction Counter, and publication of this information does not convey any rights to reproduce it or to use it for any purpose other than in connection with the installation, operation, and maintenance of the equipment described herein.

COPYRIGHT 1975 DATA PRECISION CORPORATION PRINTED IN THE U.S.A.

CONTENTS

1. INTRODUCTION
   - 1.1 General
   - 1.2 Specifications

2. OPERATION & CALIBRATION
   - 2.1 General
   - 2.2 Controls & Indicators
   - 2.3 Measure Frequency
     - 2.3.1 General
     - 2.3.2 Step-by-Step Procedure
   - 2.4 Measure Period
     - 2.4.1 General
     - 2.4.2 Step-by-Step Procedure
   - 2.5 Totalizing Events
     - 2.5.1 General
     - 2.5.2 Step-by-Step Procedure
   - 2.6 Stopwatch
     - 2.6.1 General
     - 2.6.2 Step-by-Step Procedure
   - 2.7 Options
     - **2.7.1 BCD Outputs**
     - **2.7.2 BCD Interfacing**
     - **2.7.3 Remote STOP/STOP**
     - **2.7.4 External CLOCK**
   - 2.8 Calibration
     - 2.8.1 General
     - 2.8.2 Step-by-Step Procedure

3. PRINCIPLES & THEORY OF OPERATION
   - 3.1 General
   - 3.2 Simplified Block Diagrams
     - 3.2.1 Measuring FREQUENCY
     - 3.2.2 Measuring PERIOD
     - 3.2.3 Counting Time Increments (SECONDS)
     - 3.2.4 Totalizing EVENTS
   - 3.3 Gating Controls
     - 3.3.1 Counter Gate
     - 3.3.2 Divider Gate
   - 3.4 Counter-Latch-Display Controls
     - 3.4.1 Intercycle Control (Repetitive)
     - 3.4.2 Manual Control
   - 3.5 Input Signal Conditioning
   - 3.6 Time Base Generation
   - 3.7 Programmable Divider
   - 3.8 Counter Gating
     - 3.8.1 Counter Gate
   - 3.9 Intercycle Control
     - 3.9.1 Repetitive Measurement
     - 3.9.2 Manual Measurement
   - 3.10 Counter-Latch-Overflow
   - 3.11 Display
   - 3.12 BCD Option

4. MAINTENANCE
   - 4.1 General
     - 4.1.1 Technician Qualification
   - 4.2 Trouble-Shooting Strategy
     - 4.2.1 Overall Flow Diagram
     - 4.2.2 Display Symptoms
   - 4.3 Test Equipment
   - 4.4 Overall System Performance Check
     - 4.4.1 General
     - 4.4.2 Set-Up
   - 4.5 Power Supply Check
     - 4.5.1 General
     - 4.5.2 Procedure
   - 4.6 Crystal Time Base Check
   - 4.7 Counter-Latch-Display Check
     - 4.7.1 Set-Up
     - 4.7.2 Procedure
   - 4.8 Input Signal Conditioning, Programmable Divider, and Decimal Point Check
     - 4.8.1 Set-Up
     - 4.8.2 Procedure

5. PARTS LISTS
   - 5.1 Display Assembly
   - 5.2 Main Assembly

6. REFERENCE SCHEMATICS
   - 6.1 Main PC Board
   - 6.2 Display
   - 6.3 BCD Option

ILLUSTRATIONS

2-1 Model 5740 Front Panel Controls and Indicators
2-2 Model 5740 Rear Panel
3-1 Model 5740 FREQUENCY Measurement Simplified Block Diagram
3-2 Model 5740 PERIOD Measurement Simplified Block Diagram
3-3 Model 5740 SECONDS Measurement (STOPWATCH) Simplified Block Diagram
3-4 Model 5740 EVENTS Totalizing Simplified Block Diagram
3-5 Model 5740 Input Signal Conditioning, Schematic
3-6 Model 5740 Programmable Divider, Schematic
3-7 Model 5740 Counter Gating, Schematic
3-8 Model 5740 Intercycle Control, Schematic
3-9 Model 5740 Intercycle Control, Timing Waveforms
3-10 Model 5740 High Speed LSD Timing Waveforms
4-1 Overall Trouble-Shooting Flow Diagram
4-2 Power Supply Trouble-Shooting Strategy and Test Sequence
4-3 Model 5740 Main PC Board Assembly Test Points and Components
4-4 Crystal Time Base Check Test Sequence
4-5 Input Signal Conditioning & Decimal Point Test Sequence
4-6 Input Signal Conditioning & Attenuator Test Check
4-7 Programmable Divider Test Sequence
4-8 Intercycle Control Test Sequence

COPYRIGHT 1975 DATA PRECISION CORPORATION. PRINTED IN THE U.S.A.

Frontispiece. Model 5740 Multifunction Counter

COPYRIGHT 1975 DATA PRECISION CORPORATION PRINTED IN THE U.S.A.

1

INTRODUCTION

1.1 GENERAL

Data Precision Model 5740 Multi-Function Counter is a medium-frequency, seven decimal-digit display unit, capable of operating in any one of four measurement modes. The Model 5740:

1) Measures frequencies of repetitive signals from 5Hz to 100MHz.

2) Measures periods from 0.5usec to 0.2 sec.

3) Measures time intervals from 0.01 sec to 99,999.99sec, and displays five integral decades and two decimals of the total.

4) Totalizes events from one to 9,999,999 and displays seven full decades of that total.

5) Provides four selectable time intervals from 0.01sec to 10sec over which to average the measured frequency.

6) Provides four selectable multiples from 1 to 1000 of the number of cycles over which to average the measured period.

7) Automatically positions the displayed decimal point to obtain direct readout of kilohertz (Frequency measurement), microseconds (Period measurement), hundredths of seconds (Time interval measurement), or units (Events measurement).

8) Makes its measurements with signal inputs as low as 10mV RMS (sine wave) or 30mV peak (pulse), with duty cycles as low as 10% of CW or AM modulated signals.

9) Provides a front-panel trigger level control to adjust threshold of axis crossings for low duty-cycle, offset, and AM-modulated inputs.

10) Incorporates a built-in hysteresis so that noisy input signals may be measured accurately.

11) With BCD option installed, provides four-line BCD (1-2-4-8) output data for each of the seven digits, decimal point location, and counter status signals for remote display, recording, or data processing applications. Also includes remote START-STOP control for Time measurements.

12) Has optional provision for introducing high precision external crystal-controlled time base in addition to the internal, aged-crystal controlled time base circuit.

The instrument is self-contained in one portable case only 3-1/2" high by 8-1/2" wide by 7-1/4" deep, with a carrying handle that doubles as a tilt stand. A three-wire line power cord is integral with the unit, and the power line is protected with a rear-panel accessible line fuse. All operating controls, indicators, and input connections are front-panel mounted.

Each instrument is designed for one of the standard 115 or 230V, 47 to 430 Hz power mains, and the particular source for which the instrument is wired as it leaves the factory is shown on the rear panel label.

COPYRIGHT 1975 DATA PRECISION CORPORATION. PRINTED IN THE U.S.A.

1.2 SPECIFICATIONS

1.2.1 Mode Performance

Frequency Measurement

Ranges:	Sinewave:	5Hz to 100MHz
	Pulse:	0 pps to 100,000,000 pps (Double Pulse Resolution: 15 nanosec. between consecutive pulses)
Gate Times/Resolution:		.01 sec/100Hz .1 sec/ 10Hz 1 sec/ 1Hz 10 sec/0.1Hz
Accuracy:		±1 count ± time base uncertainty
Readout:		Directly in Kilohertz (7 decimal digits)

Period Measurement

Ranges:	Sinewave:	0.5 to 200,000.0 µsec. (5Hz to 2MHz)
	Pulse:	0.5 to 9,999,999 µsec. (0 pps to 2,000,000 pps) (Max. Resolution: 1 nanosec.)
Periods Averaged/ Resolution:		1/ 1 usec. 10/ 0.1 usec. 100/ 0.01 usec. 1000/0.001 µsec.
Accuracy:		$\frac{\text{Trigger Uncertainty } (\leq 20 \text{ nanosec.})}{\text{No. of Periods Averaged}}$ + time base uncertainty ±1 count
Readout:		Directly in microseconds.

Events Totalizing

Ranges:		0 to 9,999,999 to Overflow (counting continued after overflow)
Signal:	Sinewave:	5Hz to 2MHz
	Pulse:	0 to 2M pps

"stopwatch" Seconds Measurement

Ranges:	0 to 99,999.99 seconds (27.78 Hrs.)
Resolution:	0.01 seconds

COPYRIGHT 1975 DATA PRECISION CORPORATION PRINTED IN THE U.S.A.

1.2.2 Instrument Performance

Time Base

Type:	High-Stability Crystal
Frequency:	10MHz
Uncertainty:	±0.1 ppm, Field adjustable
Stability:	±0.01 ppm/sec. (Jitter) ±0.6 ppm/month ±4.0 ppm/year
Temperature:	±5 ppm, oven $0^{\circ}C$ to $40^{\circ}C$
Power Supply Sensitivity:	< 0.1 ppm at all modes
Warm-up Time:	< 10 minutes to rated performance

Input Characteristics

Coupling: AC (RC ≃ 0.05 seconds)

Impedance: 1 Megohm || 25pf (Input 2V @ x1 Atten)
68 kilohm (Input 2V @ x1 Atten)

Sensitivity (@ x1 Atten):

- Sinewave: 10mV RMS 5Hz to 20MHz linearly to 50mV RMS @ 100MHz
- Pulse: 30mV p-p @ .25 nanosec. width linearly to 150mV p-p @ 7.5 nanosec. width
- Rise Time: for adequate sensitivity after RC= 0.05 sec. coupling
- Dwell Time: > 200 nanosec. (Period)
  5 nsec. (Freq., Events)

Trigger Level: Adjustment Range @ x1 Atten = ±0.5V
@ x20 Atten = ±10V

Maximum Inputs w/o Damage:

- Sinewave: DC to 50KHz: 250V RMS
  50KHz to 100MHz: V x F Product = 12.5×10^6 (Or 5V, whichever is the greater)
- Pulse: Peak AC + DC 500V
  (AC component limited as above)

Display

7 LED decimal digits, 0.43" high
5 LED decimal point
2 LED Annunciators (Gate, Overflow)

COPYRIGHT 1975 DATA PRECISION CORPORATION. PRINTED IN THE U.S.A.

Power, Physical, Environmental

Power: 115V, 50/60Hz, or 230V 50/60Hz, factory connected; 12 Watts

Dimensions: 3½" H x 9½" W x 7-3/4" D (without handle), or 89cm x 216cm x 185cm

Weight: 6½ lbs. (shipping), 5 lbs. (net); or 2.27kg or 2.95kg, respectively

Operating Temperature: 0°C to 40°C

Storage Temperature: -25°C to +75°C

Humidity: 0 to 80% RH, non-condensing.

COPYRIGHT 1975 DATA PRECISION CORPORATION PRINTED IN THE U.S.A.

2

OPERATION

2.1 GENERAL

Data Precision Model 5740 Electronic Counter is operated using clearly marked front panel controls and indicators. Displayed values are read out directly in engineering units of kilohertz and microseconds, and annunciator lamps indicate counter OVERFLOW and GATE operating status.

Remote display of data, counter status, gate status and user control signals (e.g. printer enable) are available from the rear panel connector when the BCD option is factory installed.

Any or all options may be installed in any one Counter configuration.

Power source for the Model 5740 Counter may be either of two universally standard levels, ... 115 or 230, (47 to 63Hz), and each instrument is factory wired for the nominal voltage expected in the area in which the instrument is to be shipped. See Paragraph for instructions to modify the connections if required for other local conditions.

2.2 CONTROLS AND INDICATORS

Figure 2-1 locates and identifies Model 5740 front panel controls and indicators.

Figure 2-2 locates and identifies Model 5740 rear panel features.

Table 2-1 describes these controls and indicators and their COUNTER functions.

– BEFORE YOU OPERATE YOUR MULTIFUNCTION COUNTER –

The Model 5740 Multifunction Counter is shipped in a protective fitted plastic container. This manual is packed in its own wrapper and is placed outside the container. It should be read very carefully before operating the counter.

Your shipment should contain:

(1) One Model 5740 Multifunction Counter, with attached line cord and power fuse
(2) Certificate of Conformance
(3) Warranty Card
(4) Authenticated Factory Acceptance Test Data Sheet
(5) One Instruction Manual, containing information of Specifications, Operating Instructions, Theory of Operation, Maintenance, Parts Lists, and Reference Schematics.

Inspect the packing case and the instrument for any signs of damage during shipment; report immediately to the carrier if any apparent damage.

COPYRIGHT 1975 DATA PRECISION CORPORATION. PRINTED IN THE U.S.A.

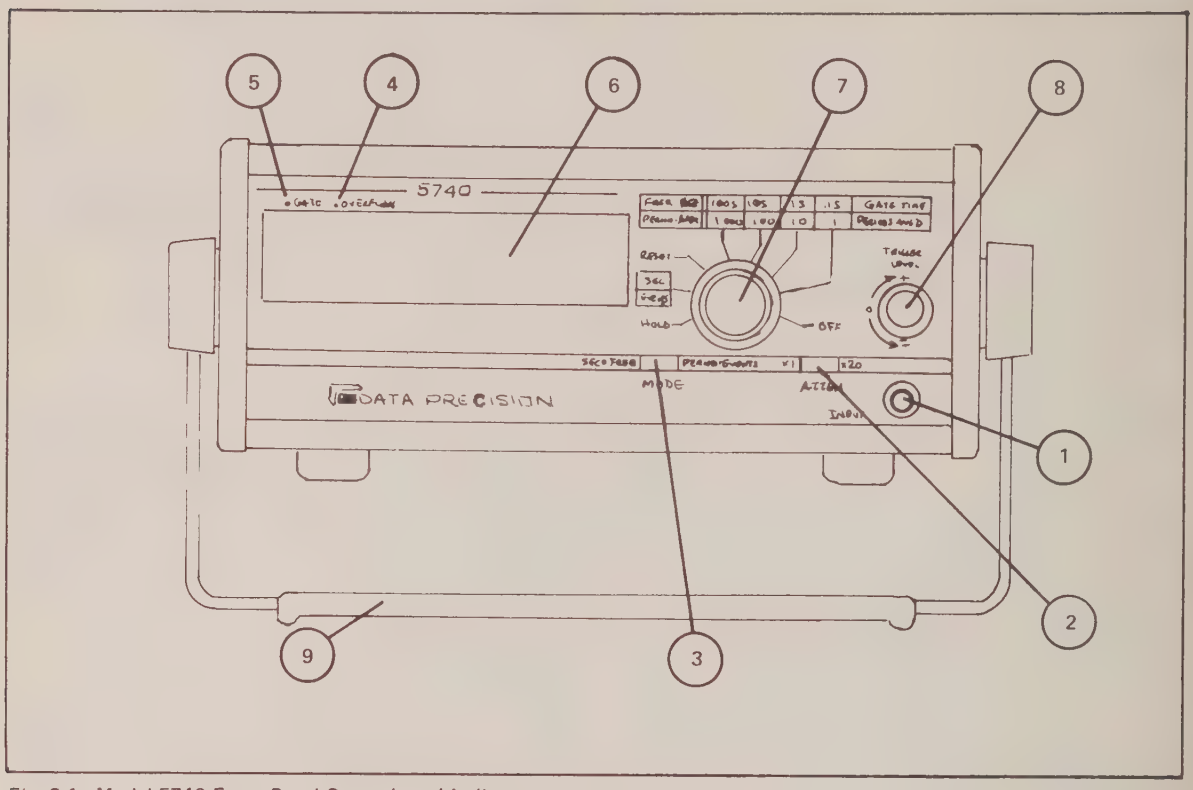


Fig. 2-1. Model 5740 Front Panel Controls and Indicators

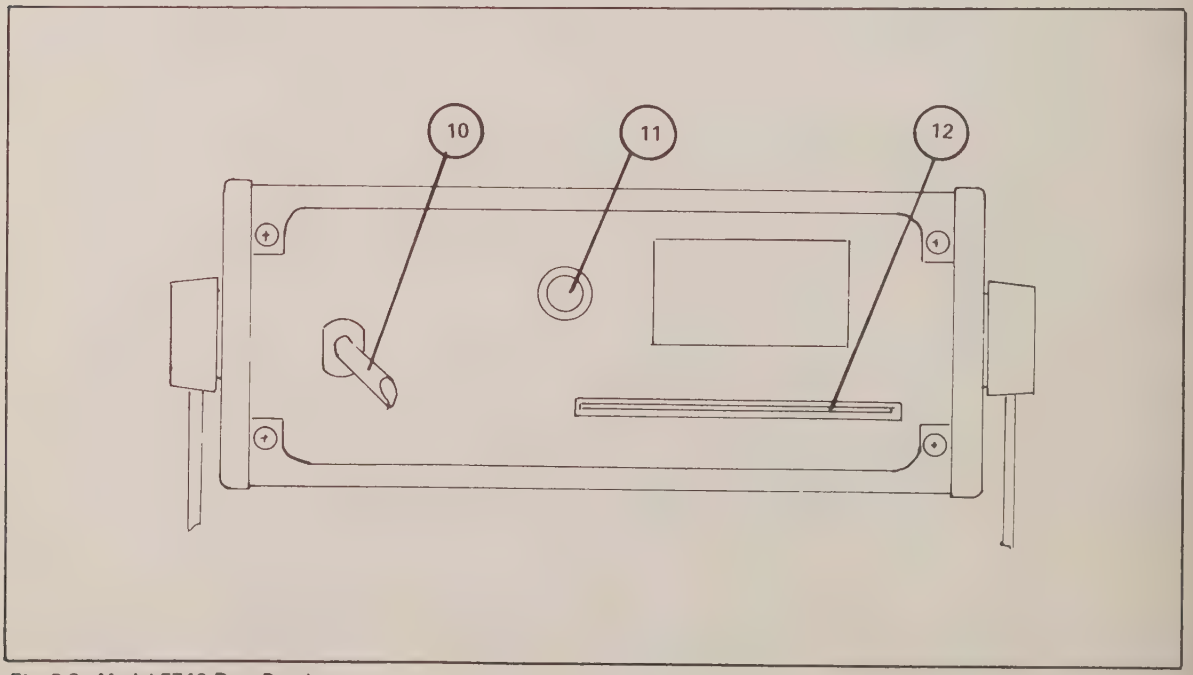


Fig. 2-2. Model 5740 Rear Panel

COPYRIGHT 1975 DATA PRECISION CORPORATION PRINTED IN THE U.S.A.

Table 2-1
MODEL 5740 OPERATING CONTROLS AND INDICATORS

REF.	NAME/DESIGNATION	DESCRIPTION & FUNCTION
1.	INPUT	BNC Connector. Connects input signal to be measured
2.	ATTEN	Two-position slide switch attenuator control. Inserts X20 or X1 attenuation of input signal.
3.	MODE	Two-position slide switch. Selects 2 of 4 modes of operation: FREQUENCY/SECONDS or PERIOD/EVENTS
4.	OVERFLOW	Indicator light in MSD display. When ON indicates count greater than 9,999,999
5.	GATE	Indicator light in display. When ON indicates an input is gated into counter.
6.	Display	Seven decimal digits and four decimal point positions 0.5" LED display.
7.	Automatic-Manual Counter Gate Control	Eight position rotary switch. Turns OFF instrument (fully clockwise). Selects one of four averaging intervals in automatic modes (FREQUENCY or PERIOD); establishes RESET-COUNT-HOLD sequence for manual measurement modes.
8.	TRIGGER	Potentiometer control adjusts Schmidt Trigger firing level to permit measurement of low duty cycle input signals.
9.	Handle	Carrying handle. Also serves as tilt stand for bench operation.
10.	Line Cord	Attached 3-wire line power cord. EIA-type plug.
11.	Fuse	1/4-amp slow blow fuse in series with primary power input.
12.	P.C. Board Connector	Used in BCD option.

2.3 MEASURE FREQUENCY

2.3.1 General

In FREQUENCY mode of operation, the Model 5740 counts axis crossings of the pulse train derived from the input signal for a selected time interval (as determined by the rotary knob setting of Gate Time). The decimal point is automatically positioned accordingly so that the display is direct reading in kilohertz.

2.3.2 Step-by-Step Procedure

a) Operate MODE switch to the SEC·FREQ position.

b) Operate the rotary switch to 1S time base.

c) Connect input to BNC connector.

d) Operate ATTEN switch to appropriate position for expected magnitude of input signal. (For inputs less than 40V, operate ATTEN to X1.)

COPYRIGHT 1975 DATA PRECISION CORPORATION. PRINTED IN THE U.S.A.

e) Set TRIGGER LEVEL for stable values on display. (Start with knob indicator at zero, or midposition.)

f) Observe OVERFLOW indicator. If ON, operate rotary switch to select lower value gate time of 0.1sec. If OVERFLOW remains ON when gate time is 0.1S, then input signal is above 100MHz specification limit.

If OVERFLOW is OFF, and if greater resolution is desired, operate rotary switch to increase gate time to 10S position. In this position, measurement will be repeated in 10.3 seconds, and least significant digit will indicate 0.1Hz increments.

g) Read display directly in kilohertz when value is stable. Table 2-2 summarizes the operation of the Model 5740 for different control settings in measuring two frequency input signals.

2.4 MEASURE PERIOD

2.4.1 General

In PERIOD Mode, the Model 5740 counts time increments for a number of pulses determined by the axis crossings of the input signal and as selected by the operation of the front panel rotary switch. The decimal point is automatically positioned so that the displayed period or average period value may be read directly in microseconds.

2.4.2 Step-by-Step Procedure

a) Operate the MODE slide switch to PERIOD·EVENTS.

b) Operate rotary switch to 100 (100 periods to be averaged.)

Table 2-2

MODEL 5740 FREQUENCY MEASUREMENT PARAMETERS

Input Frequency MHz	GATE TIME Settling Time Gate is open	Display Resolution (LSD)	Overflow	Display*
1.2345678	10 sec	.1Hz	ON	234.5678
	1 sec	1Hz	OFF	1234.567
	.1 sec	10Hz	OFF	01234.56
	.01 sec	100Hz	OFF	001234.5
99.999990	10 sec	.1Hz	ON	999.9900
	1 sec	1Hz	ON	9999.990
	100 msec	10Hz	OFF	99999.99
	10 msec	100Hz	OFF	099999.9

*For greatest resolution, use Time Base setting for minimum number of leading zero's without OVERFLOW.

COPYRIGHT 1975 DATA PRECISION CORPORATION PRINTED IN THE U.S.A.

Table 2-3

MODEL 5740 PERIOD MEASUREMENT PARAMETERS

Input Period Micro-Seconds	No. of Input Cycles Gate Was Open	Resolution (LSD)	Overflow Light	Display*
123456.00	1	1 us	OFF	0123456
	10	.1 us	OFF	123456.0
≈8.1Hz	100	.01 us	ON	23456.00
	1000	.001 us	ON	3456.000

*Select resolution position for non-overflow reading with minimum leading zero's.

c) Connect input to BNC connector.

d) Operate ATTEN to appropriate position for expected magnitude of input signal. (For inputs less than 40V, ATTEN = X1.)

e) Set TRIGGER LEVEL for stable values on display. (Start with knob indicator at zero, or midposition.)

f) Observe OVERFLOW indicator. If ON, operate rotary switch to select lesser number, 10, of periods to be averaged; if OVERFLOW is still ON, rotate switch to select least number, 1, of periods to be averaged. If still in OVERFLOW, Period is greater than 9,999,999usec (or 10 sec), and if sine wave, then input is not within specified value.

g) Read display directly in microseconds, when displayed value is stable.

Table 2-3 summarizes the operation of Model 5740 for different control settings when measuring an input period corresponding to approximately 8Hz.

2.5 TOTALIZING EVENTS

2.5.1 General

In the EVENTS mode of operation, the Model 5740 counts axis crossings of the input signal over a time interval determined by the manual operation of the front panel rotary control knob (or by electrical control signals when the BCD option is installed).

2.5.2 Step-by-Step Procedure

a) Operate MODE switch to PERIOD·EVENTS position

b) Operate Rotary switch to RESET position

c) Connect input to BNC front-panel connector

d) Operate ATTEN switch to appropriate position for expected input amplitude. (For inputs greater than 40 volts, operate ATTEN to X20.)

e) Operate Rotary switch to SEC·EVENTS position. The GATE light comes ON and remains ON while counting events.

f) Observe counted value as displayed. If the displayed values appear to be much more erratic than expected, then operate TRIGGER LEVEL control to stabilize the counting.

g) To stop the counting, operate the Rotary switch to the HOLD position.

h) To continue the counting from the previously held value, operate the Rotary switch to the SEC·EVENTS position.

i) To start a new events totalizing cycle begin with Step b) above.

COPYRIGHT 1975 DATA PRECISION CORPORATION. PRINTED IN THE U.S.A.

2.6 STOPWATCH

2.6.1 General

In SECONDS mode of operation, the Model 5740 is used as a STOPWATCH and counts time in increments of 0.01 seconds for an interval under manual control via the front panel rotary switch or by electrical control signals when the BCD option is installed. The displayed value is read out directly in seconds (to 0.01 sec resolution); the decimal point is correctly positioned on the display.

2.6.2 Step-by-step Procedure

a) Operate MODE slide switch to SEC·FREQ position.

b) Operate the rotary switch to RESET. This action resets the display to 00000.00. GATE Light goes OUT after display is reset.

c) To start timing, operate Rotary switch to SEC·EVENTS. GATE light comes ON and remains ON, while the least significant digit increments at 100 per second rate.

d) To stop timing, operate rotary knob to HOLD. GATE light goes OUT and display value remains at last count.

e) Read time in seconds. Maximum value is 99,999.99 seconds, or 27.8 hours, up to appearance of OVERFLOW. If greater time interval is to be counted, make note of number of counter display overflows and extend reading accordingly. For example, if there has been one OVERFLOW, the maximum value will be 199,999.99 seconds. (The OVERFLOW annunciator remains ON from moment of first OVERFLOW.)

f) To continue STOPWATCH action from the held count, operate Rotary switch to SEC·EVENTS position.

g) To start new STOPWATCH timing cycle, operate Rotary switch to RESET as in Step b) above.

2.7 OPTIONS

2.7.1 BCD Outputs

When BCD option is installed, internal circuits are modified and the main PC-board terminals are connected to counter value, operational status, and control circuitry. Terminal designations for the 44-pin edge connector are identified in Table 2-4. Note that two signals are used to identify the four operating modes, and combinations of these two for each operating mode are shown in Table 2-5.

2.7.2 BCD Output Interfacing

a) Data outputs are parallel, BCD (1, 2,4,8) and DTL/TTL compatible.

Logic "1" > +2.4V
Logic "0" < 0.4V sink for 4mA
Fanout for 2TTL loads

b) Status as identified by the terminal nomenclature is indicated by a high level (Logic "1").

2.7.3 Remote START/STOP

When the optional provision for Remote START/STOP is installed, the user may control the Counter action by applying a DTL/TTL low level or ground signal to the designated rear panel connector terminals as identified in Table 2-4.

NOTE: The remote control of the Counter must be activated ONLY when the Counter is in the SEC/EVENTS counting operation.
If in FREQ or PERIODS AVGD Mode, applying a remote control signal will stop or reset the counting in process.

a) Select SEC·EVENTS operation at the front panel.

b) Obtain the desired Counter performance by applying digital logic levels in accordance with the table below.

Counter Operation	RESET	HOLD
RESET	"0"	"1"
COUNT	"1"	"1"
HOLD	"1"	"0"

"0" = Ground or <2.5VDC or disconnected.
"1" = 3.5V±1VDC

2.7.4 External CLOCK

When the optional provision for External CLOCK is installed, the Model 5740 rear panel is modified to incorporate a BNC connector and switch. To use the external clock feature, an accurate oscillator of 10 MHz should be available.

COPYRIGHT 1975 DATA PRECISION CORPORATION PRINTED IN THE U.S.A.

a) Connect the external 10 MHz CLOCK to the rear-panel BNC connector.

b) Operate the rear panel selector switch to EXTERNAL.

NOTE: The internal clock remains installed in this option, and the user may switch to the internal clock by operating the rear panel switch to INTERNAL.

2.8 CALIBRATION

2.8.1 General

The Model 5740 COUNTER time base utilizes a crystal-controlled oscillator whose frequency is adjustable over a very narrow range by capacitor C12. If a very accurate frequency standard is available (better than .01ppm) it may be used to calibrate the Model 5740 COUNTER, using the procedure detailed in the next paragraph.

2.8.2 Step-by-Step Procedure

a) Allow 30 minute warm-up.

b) Set up the frequency standard for a signal near full scale range of the COUNTER: 10MHz on 1Hz resolution scale. Connect to COUNTER INPUT, i.e., use frequency of approximately 1, 10, or 100MHz.

c) Set up COUNTER for FREQUENCY Mode, select 1 sec gate time.

d) Remove top cover of the COUNTER; locate trim capacitor C12 (See Figure 4-3).

e) Adjust C12 until measured value is equal to the frequency standard and results in 0000.000 display plus overflow indication.

f) Remove standard; close cover; unit is recalibrated.

Table 2-4

OPTIONS: BCD & Remote START/STOP

CONNECTOR DESIGNATIONS

D4B1	1	A	D1B4
D4B2	2	B	D1B2
D4B4	3	C	D1B1
D4B8	4	D	D1B8
PRINT ENABLE	5	E	DP1
D5B1	6	F	DP5
D5B2	7	H	DP4
D5B4	8	J	DP3
D5B8	9	K	DP2
	10	L	D2B2
	11	M	D2B1
MODE(1)	12	N	
D6B1	13	P	
D6B2	14	R	MODE(1)
D6B4	15	S	D3B8
D6B8	16	T	D3B4
$\overline{\text{RESET}}$*	17	U	D2B4
D7B1	18	V	D2B8
D7B2	19	W	D3B1
D7B4	20	X	D3B2
D7B8	21	Y	OVERFLOW
GND	22	Z	$\overline{\text{HOLD}}$*

Note (1) See Table 2-5 for Mode status decoding.

*Active only when the Remote START/STOP is installed

Table 2-5

DECODING MODEL 5740 OPERATING MODE SIGNALS

TERMINAL R	TERMINAL 12 = 0	TERMINAL 12 = 1
0	FREQUENCY	SECONDS
1	PERIOD	EVENTS

"0" = Ground level; 0V, nominal
"1" = +5V, nominal

COPYRIGHT 1975 DATA PRECISION CORPORATION. PRINTED IN THE U.S.A.

CALIBRATION RECORD

DATE	BY	COMMENTS

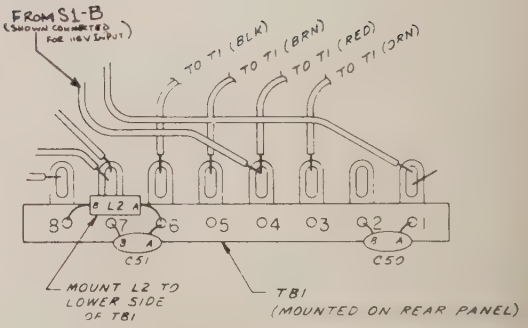
DATE	BY	COMMENTS

NOTES

CHANGING POWER SOURCE CONNECTIONS

The connections for power source voltage (100V, 115V, or 230V) are made on the Terminal Board (TB1) mounted on the inside of the rear panel, and through which the power source is switched to the appropriate input transformer tap. The table below defines the TB1 terminals to which the lead from Switch 1-B should be connected for the designated power source. The illustration at the right may be used to help identify the correct wire lead.

POWER SOURCE	100VAC	115VAC	230VAC
CONNECT S1-B to	TB1-5	TB1-4	TB1-3



COPYRIGHT 1975 DATA PRECISION CORPORATION PRINTED IN THE U.S.A.

3

THEORY and PRINCIPLES of OPERATION

3.1 GENERAL

The Model 5740 MULTIFUNCTION ELECTRONIC COUNTER comprises a counter-latching register-display chain, an input signal conditioning circuit, a crystal-controlled time base, programmable digital control circuitry, and the necessary regulated and filtered power supplies. Operation of two front panel switches sets up the instrument for one of four measuring modes. The 5740:

Measures FREQUENCY of Input Signal in Kilohertz

Measures PERIOD of Input Signal in Microseconds

Counts Time in SECONDS

Totalizes EVENTS in Units

Operation of the instrument for each function is explained with the aid of simplified block diagrams for each function. Complete schematics are reproduced and bound in the rear of the book and should be referenced when the theory of operation of each module of the instrument is described.

3.2 SIMPLIFIED BLOCK DIAGRAMS

3.2.1 Measuring FREQUENCY

As shown in Figure 3-1, when slide switch S4 is in the SECONDS/FREQUENCY position, the input signal is gated to the Counter-Latch-Display chain, and the 1MHz time base is gated to the Programmable Divider. The selected position of rotary switch S3 sets up the divider for a GATE TIME base of 10msec, 100msec, 1sec, or 10sec, while simultaneously positioning the decimal point in the display to the appropriate decade.

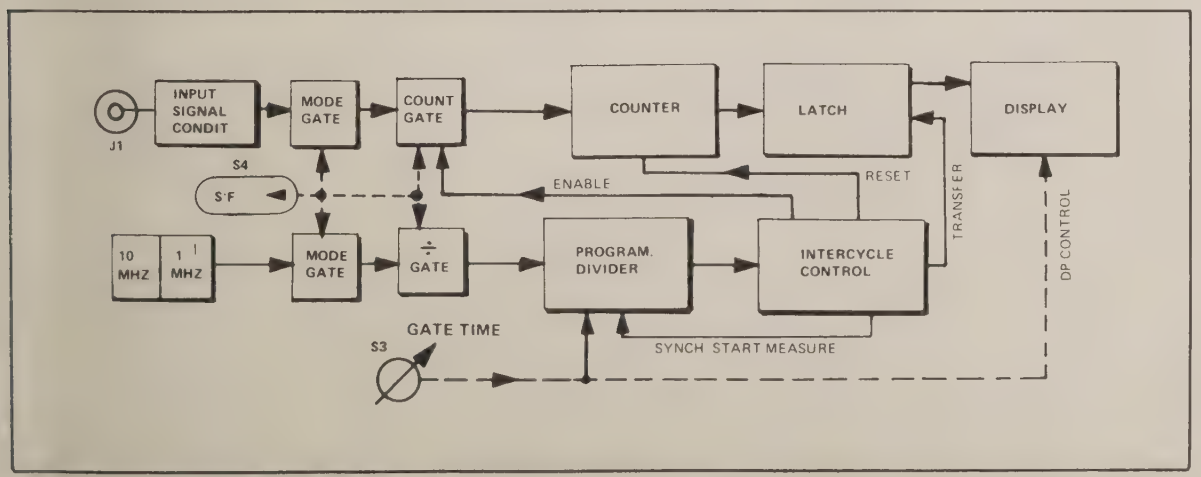


Fig. 3-1. Model 5740 FREQUENCY Measurement Simplified Block Diagram

COPYRIGHT 1975 DATA PRECISION CORPORATION. PRINTED IN THE U.S.A.

In operation, input signals of sine waves or pulse trains are converted to a TTL compatible pulse train by the input signal conditioning circuitry and gated to the counter by control signals from the intercycle control circuitry. The Programmable Divider operates on the gated 1MHz time base and counts down according to the selected GATE TIME.

At the end of the selected GATE TIME interval, the Intercycle Control Circuitry removes the enabling level from the Counter Gate, thereby stopping the counter. At the same time, a three-step counter in the Intercycle Control generates control signals to:

1) Transfer the value from the Counter to a Latching Register which automatically updates the Display,

2) Reset the Counter in preparation for the next conversion cycle and,

3) Initiate the next conversion cycle by enabling the counter gate.

The sequence of control actions is accomplished in approximately 0.3 sec.

3.2.2 Measuring PERIOD

As shown in Figure 3-2, when slide switch S4 is moved to the PERIOD position, the input signal is gated to the Programmable Divider and the 1MHz time base pulse train is gated to the Counter-Latch-Display. Rotary switch S3 is used to select the number of periods of input signal counted down before transmitting a control indicator to the Intercycle Control circuitry. The Counter Gate is enabled for a selected number of input signal transitions (Periods) under control of the Intercycle Control circuit. As before, the Intercycle Control circuitry steps the value from the Counter to the Latch and thence to the Display, and sequences the circuit through RESET and the start of the next measurement cycle. The interval between such measurements is similarly approximately 0.3 sec.

3.2.3 Counting Time Increments (SECONDS)

As shown in Figure 3-3, when slide switch S4 is placed in SECONDS operation, the 1MHz time base signal is gated into the Programmable Divider which, in turn, is programmed to divide by 10,000, so that a timing signal pulse train of 0.01 seconds interval is developed at its output and connected to the Counter Gate. The Counter Gate is controlled by the action of rotary switch S3 which bypasses the Intercycle Counter programming control. At all times the Counter output is transferred to the Latching register and continuously updates the Display.

The Divider-to-Counter Gate is enabled whenever Switch S3 is in the SEC/EVENTS position, permitting the time increments to accumulate. When S3 is placed in the HOLD position, the enable level is removed from the Counter Gate, and the count value remains. Returning S3 to the SEC/EVENTS position restores the enable level to the Counter Gate and the value in the counter

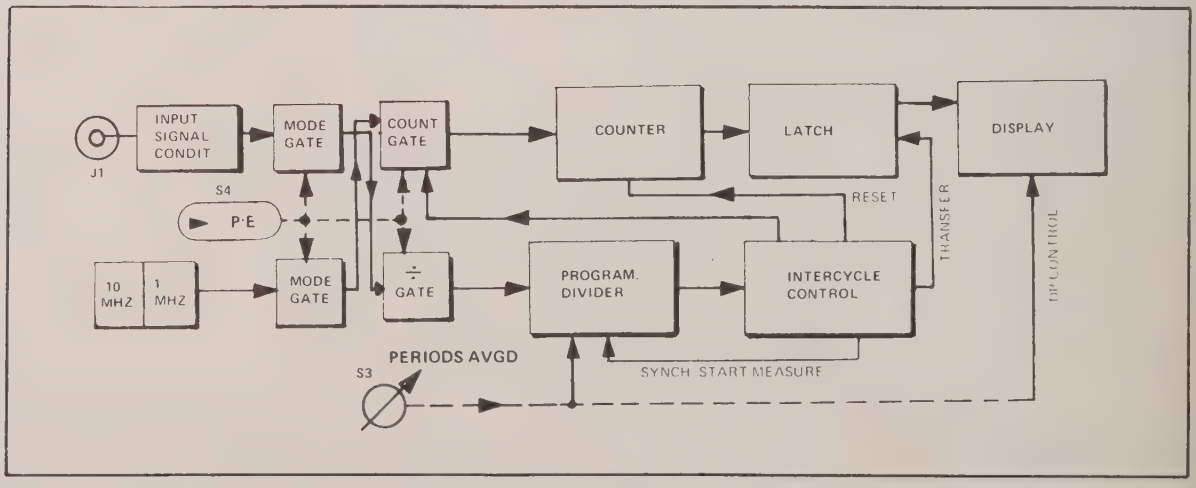


Fig. 3-2. Model 5740 PERIOD Measurement Simplified Block Diagram

COPYRIGHT 1975 DATA PRECISION CORPORATION PRINTED IN THE U.S.A.

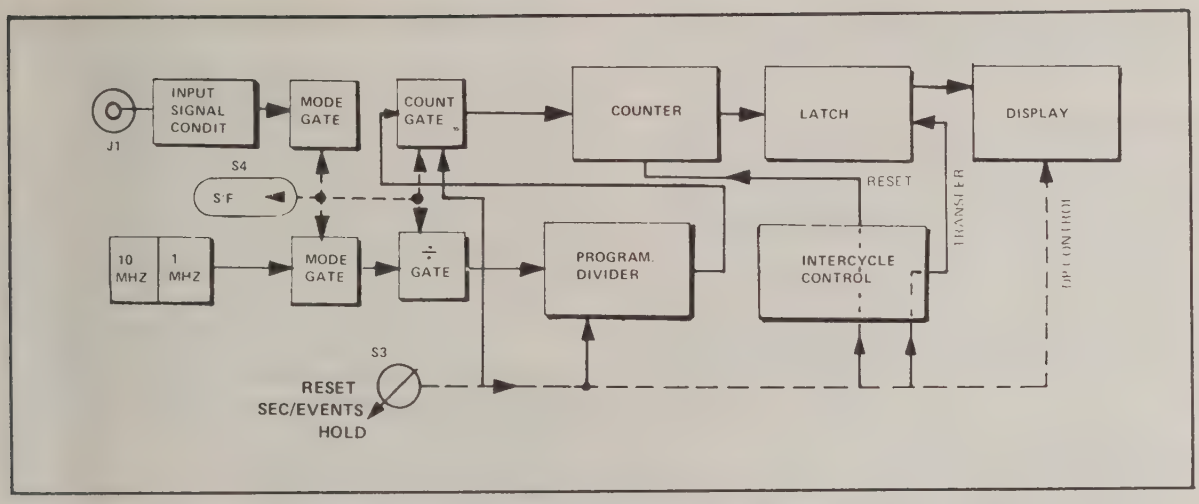


Fig. 3-3. Model 5740 SECONDS Measurement (STOPWATCH) Simplified Block Diagram

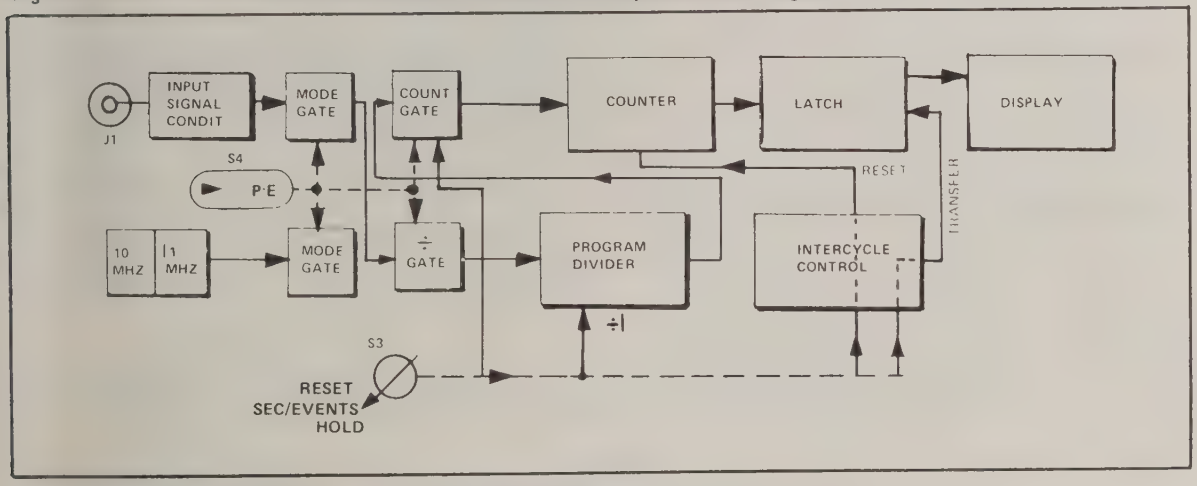


Fig. 3-4. Model 5740 EVENTS Totalizing Simplified Block Diagram

increases at the 100/sec rate from its previous value. Or the value can be reset to zero at any time by positioning the Rotary Switch to RESET position.

3.2.4 Totalizing EVENTS

As shown in Figure 3-4, when slide switch S4 is placed in the SECONDS/EVENTS position and rotary switch S3 is in any of the three manual positions, the input pulse train of events is gated to the Programmable Divider, which, in turn, is set up to divide by 1, thereby providing a pulse output for every event pulse input. As in STOPWATCH Operation, the COUNTER output is continuously transferred by the latching register and thence to the Display.

The rotary switch is operated manually in the same way as in the SECONDS Mode, enabling the Counter Gate when in the SEC/EVENTS position, holding the total count when in HOLD, resuming the totalizing count when returned to the SEC/EVENTS position, and resetting to zero at the RESET position.

3.3 GATING CONTROLS

As described in the previous paragraphs, the functions of the Model 5740 instrument are accomplished by internally programming the Counter and Divider according to the function selected by the combined settings of slide switch S4 and rotary switch S3.

COPYRIGHT 1975 DATA PRECISION CORPORATION. PRINTED IN THE U.S.A.

A summary of the front panel control matrix is shown in Table 3-1 below.

3.3.1 Counter Gate

The Counter Gate is programmed to select one of three inputs:

Conditioned Input (FREQUENCY MODE)

1MHz Time Base (PERIOD MODE)

Divider Output (.01 sec increments in (SECONDS MODE) and in (EVENTS MODE)

3.3.2 Divider Gate

The Programmable Divider Gate selects one of two inputs:

Conditioned Input (PERIOD, EVENTS MODES)

1MHz Time Base (FREQUENCY, SECONDS MODES)

3.4 COUNTER–LATCH–DISPLAY CONTROLS

Operation of the decimal point in the seven-digit display is also programmed according to the function selected by the combined settings of slide switch S4 and rotary switch S3. A summary of these control requirements is also in Table 3-1.

3.4.1 Intercycle Control (Repetitive Modes)

When measuring FREQUENCY of a repetitive input, or the PERIOD of one cycle of such an input, the Counter-Latch-Display sequence is programmed by the Intercycle Control timer. At the end of the switch-selected time base (FREQUENCY) or switch-selected number of periods (PERIOD), counter control is transferred to the Intercycle Control circuitry which

* Removes the input to the counter

* Transfers the counter value to the latching register, and thence to the display

* Resets the counter to zero

3.4.2 Manual Control

When counting SECONDS, or totalizing EVENTS, the Counter-Latch Display is programmed by the RESET-SEC/EVENTS-HOLD position of rotary switch S3. The RESET position:

* Removes the input to the counter

* Resets the counter value to zero

When operated to the SEC/EVENTS position, the control signals:

* Enable the COUNTER Gate

* Enable the transfer from Counter to Latch to Display

Table 3-1

MODEL 5740 COUNTER GATING CONTROL

MEASURING FUNCTION	Input To Counter Gate	Input To Divider Gate	Divider Ratio	Decimal Point Selection
FREQUENCY	Conditioned Input	1MHz Time Base	Selected GATE TIME	Per Selection
PERIOD	1MHz Time Base	Conditioned Input	Selected Number of PRDS AVGD	
SECONDS	Divider Output	1MHz Time Base	÷ 104 =0.01 sec Interval	DP3
EVENTS	Divider Output	Conditioned Input	÷1	None

COPYRIGHT 1975 DATA PRECISION CORPORATION PRINTED IN THE U.S.A.

When operated to the HOLD position, the control signals:

* Remove the input to the counter

3.5 INPUT SIGNAL CONDITIONING

As shown in the simplified block and circuit schematic of Figure 3-5, the signal connected at the Input J1 is transformed into a TTL-compatible pulse train via a selectable attenuator, transistor follower, threshold level control, two stages of amplification, a Schmitt trigger amplifier stage, and a level conversion stage for TTL compatibility. The conditioning circuitry also includes a clamping circuit to keep the amplifier input to ±2V peak.

The input is capacitive coupled to the resistive voltage divider (tuned by capacitors C2, C3 and C4), from which the attenuator slide switch S2 connects either about 95% (957/1025) or 47% (47/1025) of the input to high input impedance transistor follower Q1. The input to the transistor stage is clamped by CR1-CR4 to a level of ±2V. Note that the input impedance remains at about 1 Megohm (1025K) until the clamping action becomes operative, and that R1 keeps the impedance at not less than 68K ohms even when the signal is clamped by CR1-CR4.

The AC signal is capacitive-coupled to two stages of wide band amplification, followed by a third stage connected as a Schmitt trigger circuit. All three stages are part of the monolithic chip Z11. In order to obtain reliable performance of the trigger circuit where input signals have a very low duty cycle, the average value of the input may be adjusted by the front panel threshold control, R36. Because input pulse trains of very low duty cycles will have near-zero average values, the swing through zero in one direction will be of very limited amplitude (see sketch in Figure 3-5) and may not be adequate for the operation of the Schmitt trigger. The threshold level adjust circuit provides the capability to move the average level as required in order to obtain a reliable zero-crossing detection by the Schmitt trigger circuit.

The Schmitt trigger circuit incorporates a hysteresis characteristic in the trigger level circuit for more accurate waveform measurement in the presence of noise. Transistor Q2, along with gate

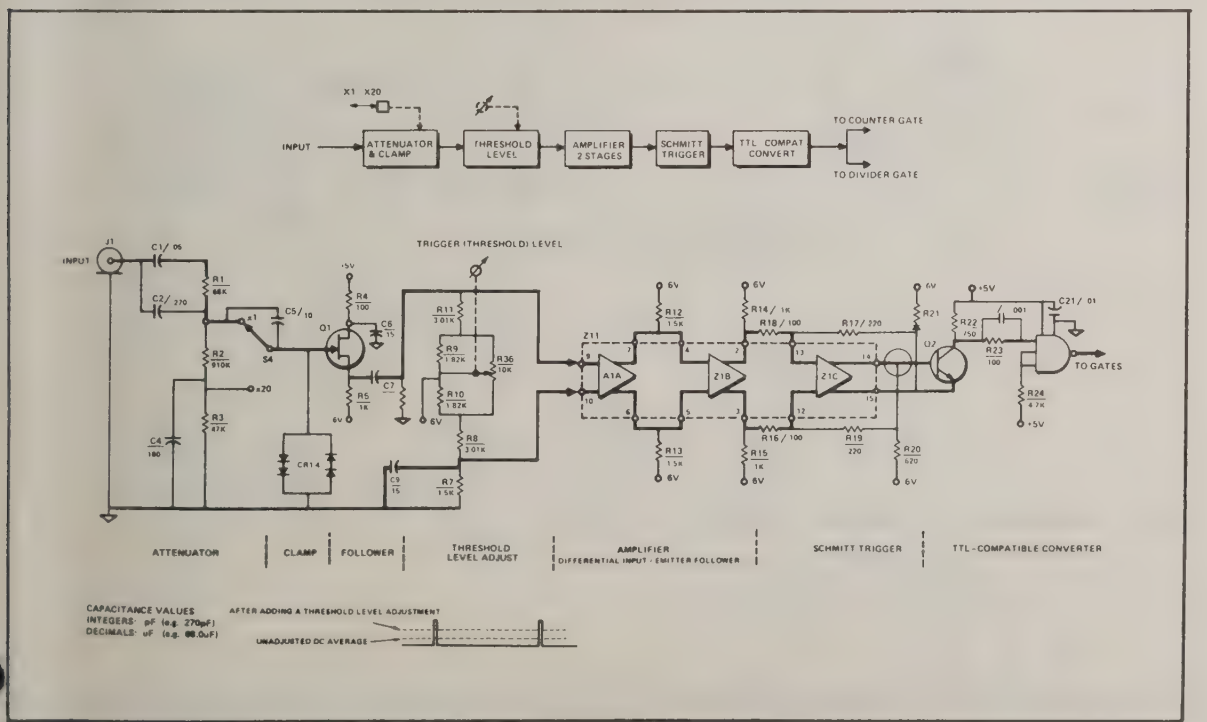


Fig. 3-5. Model 5740 Input Signal Conditioning, Schematic

COPYRIGHT 1975 DATA PRECISION CORPORATION. PRINTED IN THE U.S.A.

Z15-2, converts the amplifier chain output to TTL compatible levels for Counter or Divider processing.

3.6 TIME BASE GENERATION (FIG. 6-1)

As shown in the reference schematic, the internal time base generator consists of a precise crystal-controlled 10MHz oscillator, counted down to a 1MHz square wave. The 10MHz crystal Y1, tuned by trimmer C12 is a precision stable time base (4ppm/year). The oscillator output is counted down by Z23, connected for division by 10, so that a 1MHz square wave is generated at the output Z23-12.

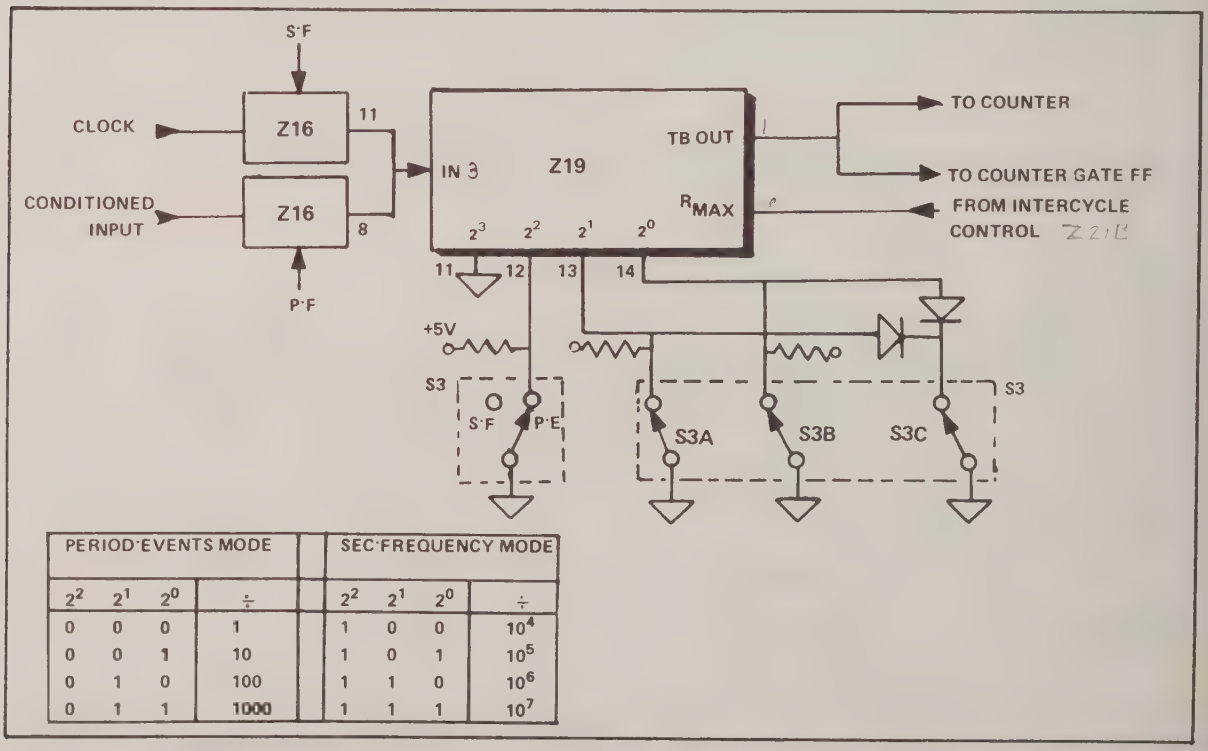
3.7 PROGRAMMABLE DIVIDER

The Programmable Divider is a monolithic IC device, Z19, which produces an output pulse (TBOUT, pin 1) for a programmed number of input pulses at pin 3, as determined by the divider ratio control signals at pins 11, 12, 13 and 14. A control signal, R_{MAX}, may be used to hold the divider interval counter at its maximum value so that the next input pulse will generate an output signal.

The Programmable Divider may have either one of two inputs, and can be programmed to divide by one of four decades. The output, TBOUT, appears at Pin 1. Figure 3-6 is a simplified block diagram illustrating the manner in which the configuration of the divider is established.

Input to the divider at Z19-3 is introduced either from Gate Z16-8 or Gate Z16-11, which are enabled by operating slide switch S4 to SEC·FREQ or PERIOD·EVENTS, respectively. The countdown division factor is determined by the combined action of rotary switch S3 and the position of slide switch S4.

a) When in PERIOD·EVENTS mode, the conditioned input signal is the input to Z19-3, and that input is divided by a factor according to the setting of S3. As shown, the 2^2 code is 0 for all settings, while switch S3 A & B determine the number of averaged periods, (PERIOD Measurement), whereas the manual settings (HOLD-SEC/EVENTS-RESET) at switch S3C establish code 000 for division by 10^6, thus resulting in one count for each event.



PERIOD·EVENTS MODE				SEC·FREQUENCY MODE			
2^2	2^1	2^0	÷	2^2	2^1	2^0	÷
0	0	0	1	1	0	0	10^4
0	0	1	10	1	0	1	10^5
0	1	0	100	1	1	0	10^6
0	1	1	1000	1	1	1	10^7

Fig. 3-6. Model 5740 Programmable Divider, Schematic

COPYRIGHT 1975 DATA PRECISION CORPORATION PRINTED IN THE U.S.A.

b) When in SEC·FREQ mode, the clock train of 1MHz pulses is the input to Z Z19-3, and S3A and S3B determine the time over which the frequency of the input signal is averaged. S4 establishes a code of 1 for Divider input 2^2 for all settings, while S3 A & B schematically select the particular averaging time interval. In manual operation, the divider factor is 10^4, providing a scale of .01 seconds per count ($10^6 \div 10^4 = 10^2$) at the divider Time Base output Z19-1.

NOTE Rotary switch S3 is shown schematically in these illustrations; the actual switch has only two wafers and uses eight positions of a 12-position configuration.

3.8 COUNTER GATING

Figure 3-7 illustrates the manner in which the Counter-Latch-Display chain is controlled in each of the four measurement functions. As described previously, the Counter is programmed to count either a pulse train derived from the divided time base (SECONDS), the 1MHz time base (PERIOD), conditioned input (FREQUENCY), or conditioned input (EVENTS). Paragraph 3.7 has described the control over the Programmable Divider, while Figure 3-7 incorporates some aspects of Intercycle Control programming as well as the gating to the counter.

3.8.1 Counter Gate

The configuration of NAND gates Z15-6, Z15-8, Z18-6 and Z18-8, inverter Z17-8 and the switches S3 and S4 comprise the functional unit referred to previously as the "Counter Gate" (See Figures 3-1, 3-2, 3-3 and 3-4). This counter gate determines what will be counted, while as shown in Figure 3-7, the GATE FF determines when the counter can count its input by placing an enabling level on the first stage of the counter high speed LSD count register. The operation of the GATE FF is determined by rotary switch S3 when in the manual functions (SECONDS, EVENTS), or by the Intercycle Control when in the repetitive functions (FREQUENCY, PERIOD).

The Programmable Divider is set to its maximum count in the interval between measurements by a high level input to terminal 6, R_{MAX}. This level is developed by GATE Flip Flop Z21B and is programmed manually by rotary switch S3 or automatically by the Intercycle Control cir-

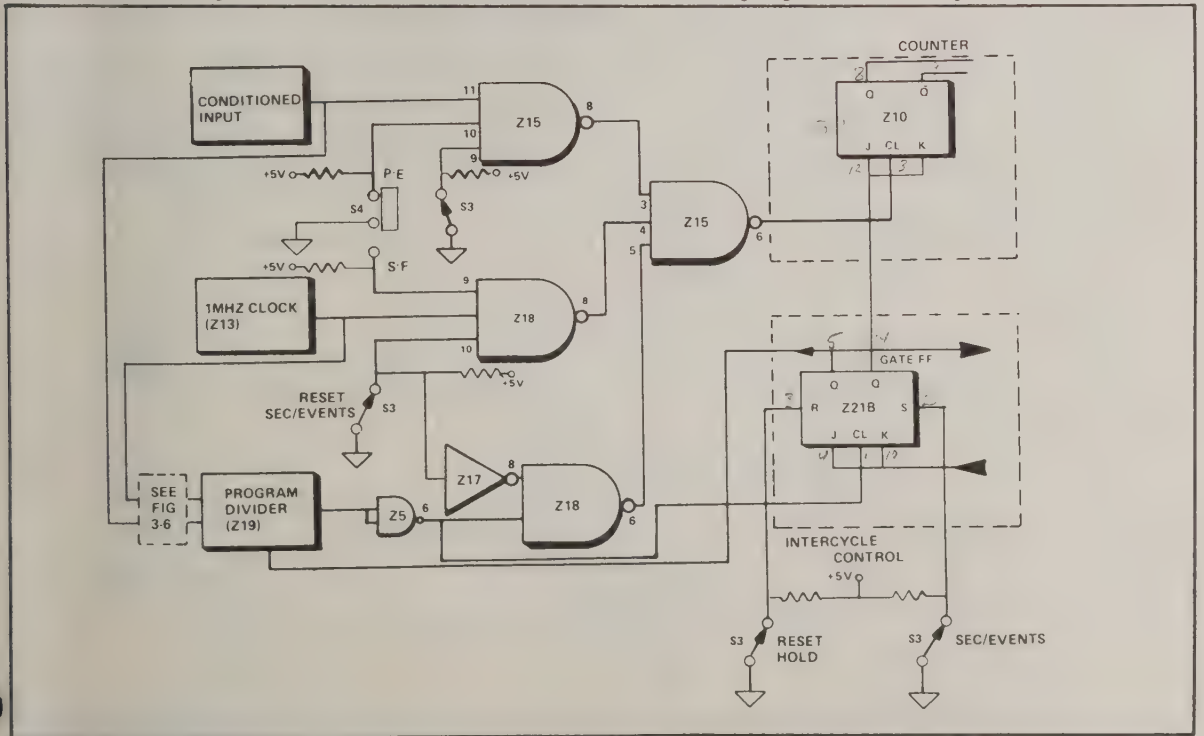


Fig. 3-7. Model 5740 Counter Gating, Schematic

COPYRIGHT 1975 DATA PRECISION CORPORATION. PRINTED IN THE U.S.A.

cuitry. The high R_{MAX} level holds the programmable divider in its full register count so that the next measurement cycle begins with the first clock pulse or conditioned input pulse after removal of the R_{MAX} high level input at Z19-6.

3.9 INTERCYCLE CONTROL

As shown in Figure 3-8, the Intercycle Control consists of an intercycle oscillator (about 0.08 sec period), two flip-flops connected as a counter, and three gates that sense the counter states.

The Intercycle Control outputs: 1) transfer the counter value to the latching register, 2) reset the counter to zero, and 3) keep the programmable divider at R_{MAX} until the display is updated and the counter is zeroed. These outputs are developed under control of the intercycle oscillator when measuring Frequency or measuring Period, or by settings of the rotary switch when in any of the manual measurement modes (Seconds or Events).

3.9.1 Repetitive Measurement

At the end of a measurement cycle in repetitive measuring modes, the Gate FF receives a clock pulse from the programmable divider Z19-1, and its $\overline{Q}$ level becomes high. [It remains high until the sense gate Z16-3 next senses the zero-zero state of the intercycle counter (to enable the Gate FF) and the next input pulse to the divider produces a clock pulse to the Gate FF.] The sequence of actions initiated when the change in Gate FF $\overline{Q}$ level to high state are described with reference to timing diagram shown in Figure 3-10.

The intercycle oscillator is a relaxation type whose period is determined by the charging path time constant of R31C31 (∿.08 sec) attempting to charge C31 to +5 volts, and the firing level of unijunction transistor Q4 set by voltage divider R32 R33 = 3V. The result is a pulse train at TP4 of about 0.08 sec period.

The Intercycle Counter is first actuated by the change in level of Z21B ($\overline{Q}$), and this change in output state produces a high level at Z16-3, initiating the charge cycle of the oscillator and setting the programmable divider to R_{MAX}. Succeeding changes in states of the counter are produced by the pulse train through Z22-11 caused by the intercycle oscillator pulses at the Z22-11 input (TP4).

The output control signals of TRANSFER and RESET are produced in sequence as shown in Figure 3-9.

When the Intercycle Counter reaches the 00 state, (both $\overline{Q}$ = 1), sense gate Z16-3 goes low, removing the constraint on R_{MAX} of the divider. After inversion through Z17-2, this control enables Gate FF JK,

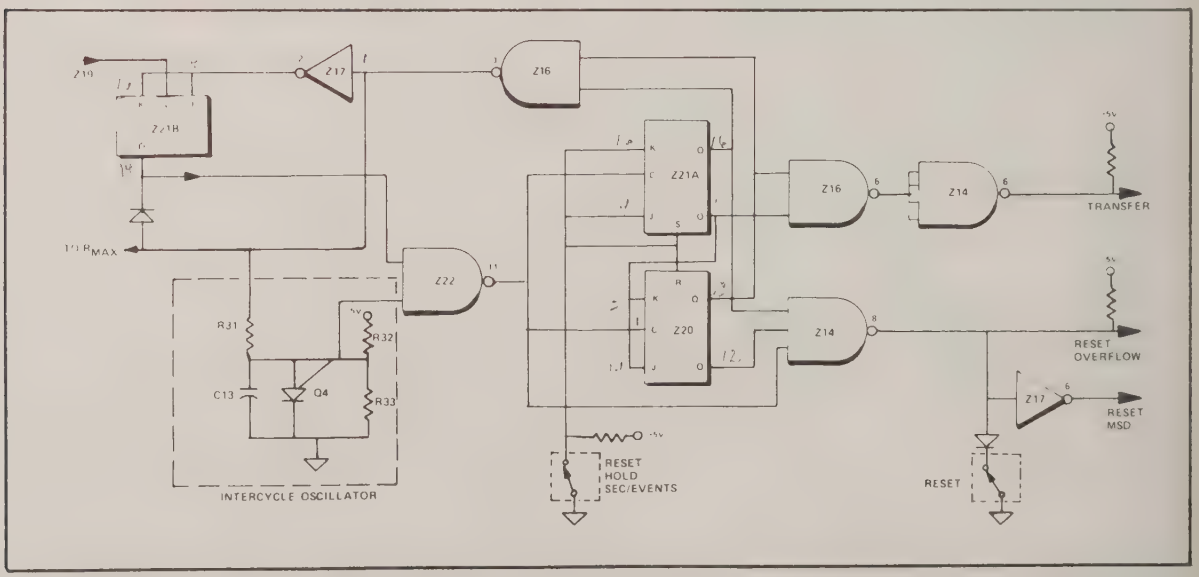


Fig. 3-8. Model 5740 Intercycle Control, Schematic

COPYRIGHT 1975 DATA PRECISION CORPORATION PRINTED IN THE U.S.A.

stopping the intercycle oscillator action. Then, after, the first divider output pulse, Z21B changes state and maintains these conditions until the succeeding Z19-1 (TB) pulse is received, signifying end of measurement.

Table 3-2 describes the flip-flop states as they respond to the control pulses from the measuring chain and the intercycle oscillator.

3.9.2 Manual Measurement

In Manual Control of the measuring process, the states of the counter flip-flops are manually SET and RESET respectively to keep a continuous TRANSFER action while rotary switch S3 is in the HOLD or COUNT or RESET positions. The RESET position of the rotary switch manually places a zero level at the output of Z14-8, accomplishing the same RESET action as in the repetitive operation of the counter.

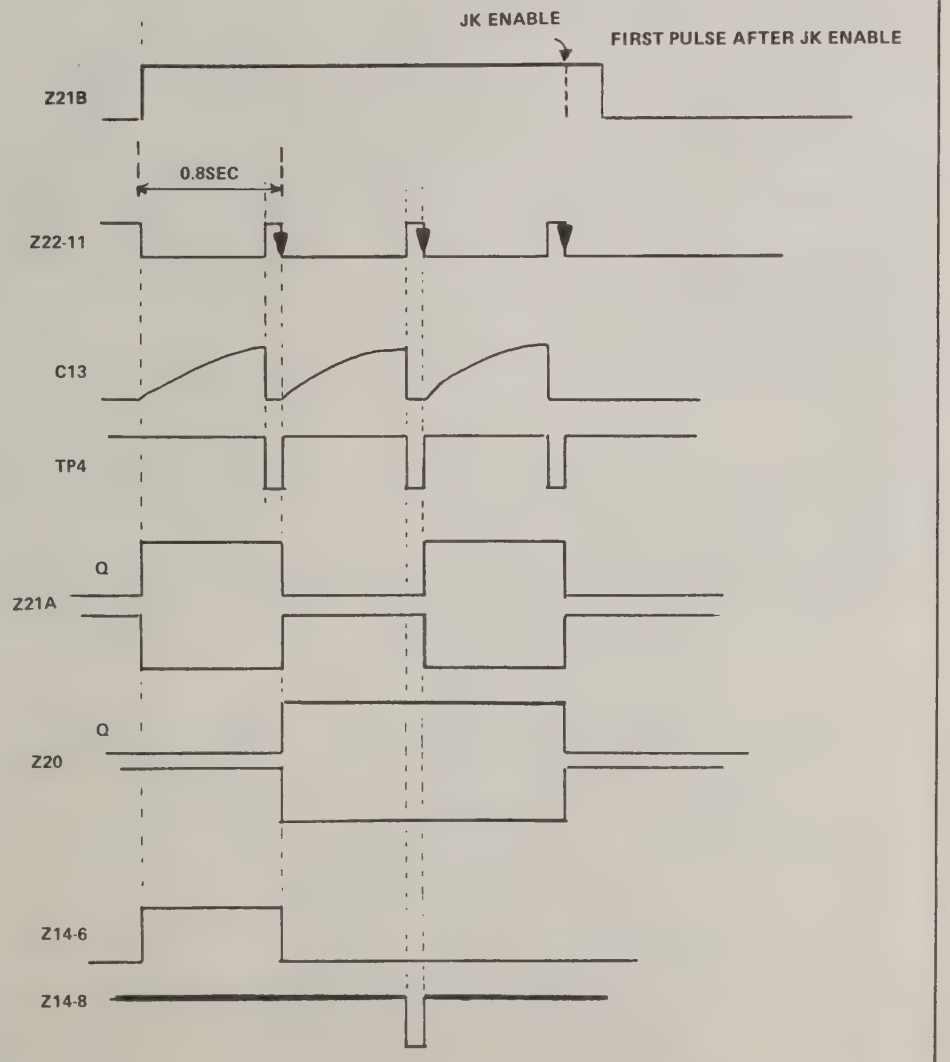


Fig. 3-9. Model 5740 Intercycle Control, Timing Waveforms

COPYRIGHT 1975 DATA PRECISION CORPORATION. PRINTED IN THE U.S.A.

Table 3-2

INTERCYCLE CONTROL LOGIC STATES

MEASURE FREQUENCY or MEASURE PERIOD

Event Action	Flip-Flop Logic Status						COUNTER	LATCH	DISPLAY
	Z21A		Z20		Z21B GATE FF		RESET $(Q \cdot \overline{Q}) \cdot$ CLOCK	TRANSFER $(Q \cdot \overline{Q})$	
	Q	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$			
At End of Previous INTERCYCLE	0	1	0	1	0 JK ENABLE	1	Ready	Latched	Static
At First CARRY Pulse out of DIVIDER Start present Measurement Cycle	0	1	0	1	1	0	Counting	Latched	Static
At Next CARRY Pulse out of DIVIDER End Measurement Start Intertercycle Osc Reset DIVIDER to R_{MAX}	1	0	0	1	0	1	Held At Current Count	Start Transfer of Counter to Latch	Start Display Update
At First Intercycle Osc Pulse	0	1	1	0	1	0	Held At Current Count	End Transfer	End Display Update
At End of Second Intercycle Osc Pulse	1	0	1	0	1	0	RESET To Zero	Latched	Last Meas Updated
At End of Third Intercycle Osc Pulse	0	1	0	1	0 JK ENABLE	1			

COPYRIGHT 1975 DATA PRECISION CORPORATION PRINTED IN THE U.S.A.

3.10 COUNTER–LATCH–OVERFLOW

The Counter, Latch and Overflow circuits are illustrated in the reference schematic. The chain is enabled by the high level from the GATE FF, and the gated counter input is selected as described in previous paragraphs.

The counter consists of a hi-speed least significant digit configuration of dual flip-flops Z8 and Z9, followed by two binary-to-BCD counters Z12 and Z13 and one four-digit binary-to-BCD counter latch, and multiplexer scan oscillator (Z1). The overflow is determined by the carry from Z1 that clocks flip-flop Z20, and is latched in the combination of gates Z22-6, Z22-8, and inverters Z17-10 and Z17-12.

The Hi-Speed LSD counter utilizes a gating combination of flip-flop outputs to convert the sequence to the valid BCD code and a carry at each tenth count. Figure 3-10 illustrates the timing and gating performed by the Binary-to-BCD conversion block in the least significant digit.

Counters Z12 and Z13 are integrated circuits that incorporate the required binary-to-BCD conversion. Individual latches Z6, Z7, and Z8 are used for the three less significant digits, while the four-decade counter Z1 incorporates both the conversion and latch.

The seven decimal digits of the measured value are multiplexed from the latches and are transmitted on two simultaneous lines: one line carries the BCD value of the three less significant digits, while the other carries the four more significant ones. The multiplexing digit address is carried on independent lines, and one line is used to identify one of the three lesser and one of the four more significant digits in the measured value.

Transfer to the latches is enabled by a control signal from Z14-6 whose generation has been described earlier. Resetting the counter requires two different levels: a low level enabling signal for the three less significant digits, and a high level for the enabling action in Z1 for the four more significant digits. The output of Z14-8 is the required low level, while the inversion through Z17-6 provides the necessary high level for Z1.

When an overflow of the counter occurs, it is sensed in flip-flop Z20 and held there until it is transferred to the display by gating action of the TRANSFER signal from Z14-6. The RESET control signal returns Z20 to the zero state.

3.11 DISPLAY

The display assembly is constructed on a separate PC board, and, as shown in the

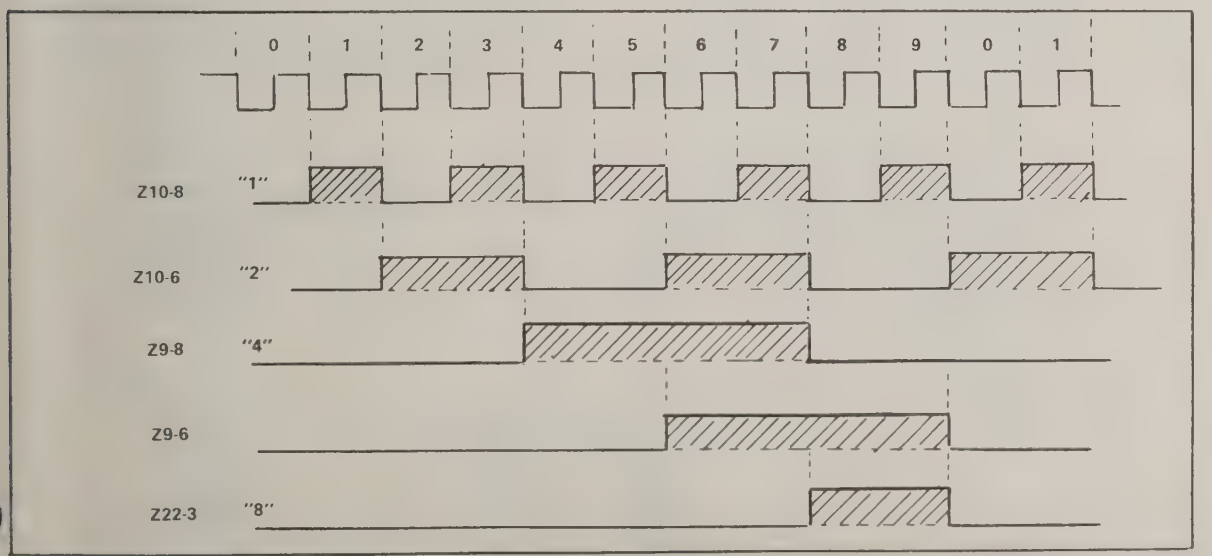


Fig. 3-10. Model 5740 High Speed LSD Timing Waveforms

COPYRIGHT 1975 DATA PRECISION CORPORATION. PRINTED IN THE U.S.A.

reference schematic, includes 7 one-digit display units, four anode-driver circuits that are gated with the digit select control signal of the multiplexer, two BCD-to-seven segment converters for the groups of digit data transmitted from the main assembly, resistor-coupled ground signal for the selected decimal point, and transistor drivers for the OVERFLOW and GATE annunciators. Note that the decimal points of the two more significant digits (not used as decimal points) are used as the annunciators in the upper left (instead of lower right) location. This inverted position of the display is compensated for by suitable selection of the seven segments to display the desired digit.

3.12 BCD OPTION

When BCD option is installed, the measured value in the latching registers are connected to the PC board edge terminals. In addition, certain status and control signals are also connected to the PC board to provide user capability for interpreting the values and for printing only when the value has been latched between measurements.

As shown in Drawing 75-1005 and the main reference schematic, the BCD values for the three less significant digits are available at their respective latches and are connected directly to the output terminals. The four more significant digits are de-multiplexed and transferred to independent latches Z201 to Z204 in the BCD option components, from which they are connected to the edge terminals.

Decimal point indicator signals are developed by the rotary switch action, and a ground level at any position selects that point. Ungrounded levels are held at +5V.

A Print-Enable status signal is developed by gating the instrument Hold and Transfer signals. The Print Enable is a low level when either the Transfer control is OFF, or when the Hold signal is ON. Thus, the user may recognize when the BCD data is static during the Automatic measuring modes, or during the manual measuring modes, respectively.

COPYRIGHT 1976 DATA PRECISION CORPORATION PRINTED IN THE U.S.A.

4

MAINTENANCE

4.1 GENERAL

CAUTION

The Model 5740 Multi-Function Counter is covered by a one-year warranty, and the instrument should be referred to the factory for maintenance if required within the warranty period. (All shipping charges are paid by the purchaser). Attempts to make any extensive repairs within the warranty period may invalidate the warranty. If repairs are needed after the warranty period, only qualified technicians should attempt to effect such repairs and should use test instruments and standards calibrated within the accuracy and tolerance of the specifications.

4.1.1 Technician Qualifications

A complete understanding of the theory of operation of Model 5740 is a prerequisite for efficient trouble-shooting, repair, and recalibration of the instrument. Technical training and experience necessary to master the technical material in Chapter 3, along with hands-on experience with the operation of test equipment specified in Paragraph 4.2 are considered minimal.

4.2 TROUBLE-SHOOTING STRATEGY

4.2.1 Overall Flow Diagram

Model 5740 functional circuit grouping and the provision of (carefully) selected test-points greatly simplify the isolation of trouble to major circuitry blocks. Fault isolation within each major block is facilitated by the simplified schematics of Chapter 3, and by point-to-point measurements made with reference to the fold-in schematic at the back of the book. Replacement parts should be ordered in accordance with the lists in Chapter 5.

Figure 4-1 is a block flow diagram of a Trouble-Shooting decision tree that illustrates the sequence followed and identifies the paragraphs for the detailed instructions that follow. It should be noted that a general, over-all performance check is suggested to determine instrument operational readiness, and that a sequence of closed-case operating checks with an external signal is suggested to verify operational readiness of the major counting/measuring functions.

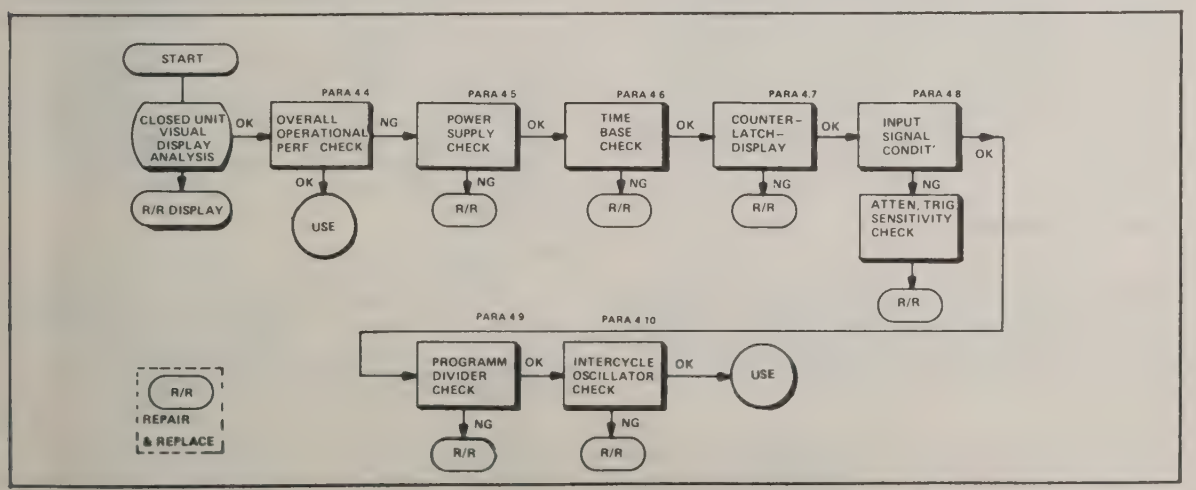


Fig. 4-1. Overall Trouble-Shooting Flow Diagram

COPYRIGHT 1975 DATA PRECISION CORPORATION. PRINTED IN THE U.S.A.

Table 4-1

TEST INSTRUMENTATION

Measure/Generate		Specifications Ranges/Accuracies	Recommended Instruments
Voltage	M	DCV: ±10V, ±100V/±0.1% ACV: 200V, 50-60Hz/±1%	Data Precision
Resistance		0-1KΩ/±1%	Model 245
Waveform Gen	G	Sine Wave: 5Hz to 100MHz	Syntest Model S1-200 (1Hz to 200MHz)
Waveform Meas	M	150MHz	Tektronix Type 454 Oscilloscope
Coupler Load	G	50-ohm	Tektronix 011-0049-01
Attenuator	G	0 to 30dB	--
Timer	G	0 to 3600 seconds/0.5 sec	--

4.2.2 Display Symptoms

Faulty display units or their decoder-drivers may be detected easily by observation and analysis of improper visual displays. For example, if a non-numeric character appears on only one digit, it is probable that the fault is in that digit or its single decoder-driver circuit. If, on the other hand, the same non-numeric character appears in a group of digits, it is probable that the fault is in the decoder-driver and associated scanning circuitry.

A/Y BOARD IS FULLY SEATED

4.3 TEST EQUIPMENT

Measuring instruments and test standards with performance specifications as listed in Table 4-1 should be used in the procedures as described in the paragraphs that follow.

4.4 OVERALL SYSTEM PERFORMANCE CHECK

4.4.1 General

This test sequence confirms the operability of the instrument in each of its four measuring modes. It checks the performance accuracy only to a wide tolerance. If any one of these tests yields an incorrect result, or if a subsequent test with accurately known inputs results in a Counter error, proceed to Paragraph 4.5, and perform the tests described therein and in subsequent paragraphs.

4.4.2 Set-Up

Use a coupling capacitor of about .01uF, 1KV to introduce a 60Hz input to the Model 5740 input, position ATTEN switch to X20, and operate the instrument as shown in Table 4-2.

[**NOTE** Use caution in coupling the line-source signal to prevent accidental short-circuiting of line power.]

COPYRIGHT 1975 DATA PRECISION CORPORATION PRINTED IN THE U.S.A.

Table 4-2

OVERALL SYSTEM PERFORMANCE CHECK (60 HZ)

S4 (Slide Switch)	S3 Manual-Auto Rotary	Display*
SECONDS/FREQ	(0.1Hz Resolution) 10S Gate	000.0600
PERIOD/EVENT	10 PERIODS AVGD 100 PERIODS AVGD	016666.6 66666.66 & Overflow
SECONDS/FREQ	RESET COUNT After 30 Seconds HOLD COUNT	00000.00 Increment at 100/sec rate 00030.00 ± 3% Continue at 100/sec rate
PERIOD/EVENT	RESET COUNT	0000000 (No D.P.) Increment at 60/sec rate

*Add ± [1 count + time base stability + line frequency stability (approx. 0.1% short term)]

4.5 POWER SUPPLY CHECK

4.5.1 General

a) All tests are made with respect to TP7

b) Non-conformance of a power supply measurement to specification may result from a power supply circuit malfunction or a malfunction in one of the driven loads. In general, a higher-than-specification value indicates a power supply malfunction, (or need for adjustment), whereas a less-than spec value may be caused by either a power supply malfunction (a need for adjustment) or load malfunction.

c) Figure 4-2 summarizes the testing strategy for isolating power supply malfunctions. See Drawing D75-1000 for circuit details, and parts list for replacement ordering information.

CAUTION

HIGH VOLTAGES ARE EXPOSED WHEN COVER IS REMOVED. OBSERVE PRECAUTIONS WHEN MAKING MEASUREMENTS WITHIN OPEN UNIT.

d) Remove top cover by first removing cover hold-down screws at rear panel. Then left cover over front-panel "dimples". All test points and component parts are identified on the top of the main PC board assembly, and are shown in Figure 4-3.

4.5.2 Procedure

Position Rotary Switch S3 to FREQ/SECONDS, and follow the measurement sequence of Figure 4-2.

4.6 CRYSTAL TIME BASE CHECK

Follow the measurement sequence of Figure 4-4.

4.7 COUNTER–LATCH–DISPLAY CHECK

4.7.1 Set-Up

Model 5740

Mode (S4): FREQ/SEC position

Rotary (S3): RESET

Timer: Set to zero

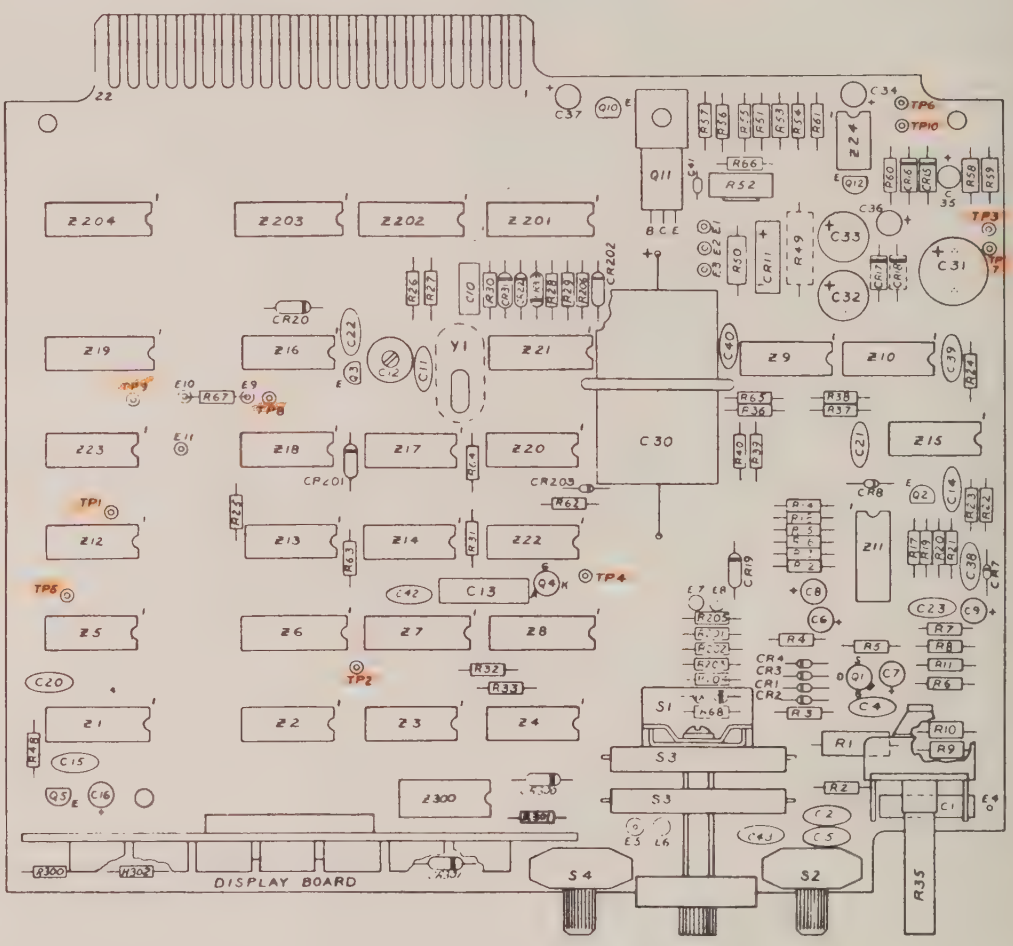
4.7.2 Procedure

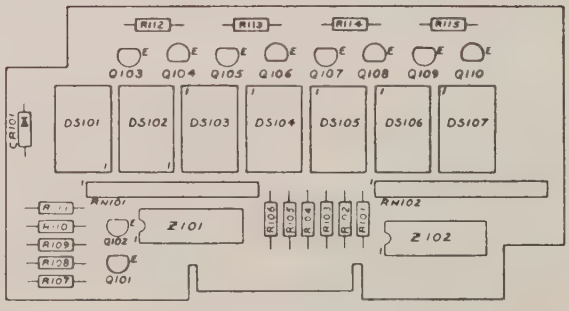
a) Simultaneously, start timer and position Model 5740 S3 to SECONDS/EVENTS

b) Observe Model 5740 display. Check to see that it tracks the value of the Timer at 10 sec, 120 sec, 180 sec, 300 sec values.

c) If apparent error, signal trace through Counter-Latch-Display chain as illustrated in reference schematic.

COPYRIGHT 1975 DATA PRECISION CORPORATION. PRINTED IN THE U.S.A.





(DISPLAY ASSEMBLY)

Fig. 4-3. Model 5740 Main PC Board Assembly Test Points and Components

COPYRIGHT 1975 DATA PRECISION CORPORATION PRINTED IN THE U.S.A.

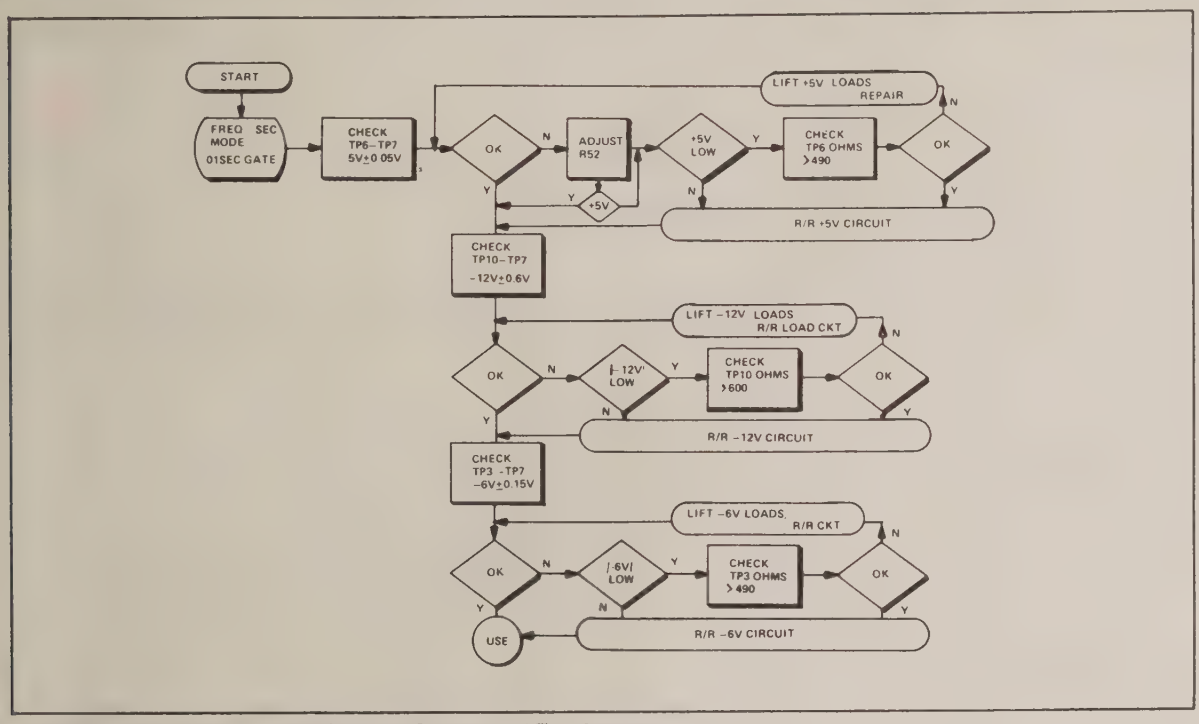


Fig. 4-2. Power Supply Trouble-Shooting Strategy and Test Sequence

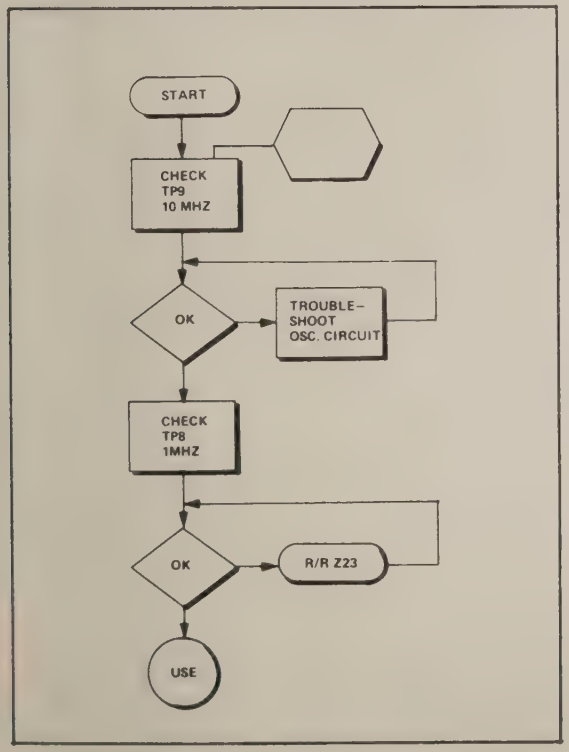


Fig. 4-4. Crystal Time Base Check Test Sequence

4.8 INPUT SIGNAL CONDITIONING; PROGRAMMABLE DIVIDER, AND DECIMAL POINT CHECK

4.8.1 Set-Up

Model 5740

ATTEN: X1

MODE Switch (S4): PERIOD/EVENTS

Rotary Switch (S3): See procedure Figure 4-5

TRIGGER Level: Mid Scale

Signal Generator

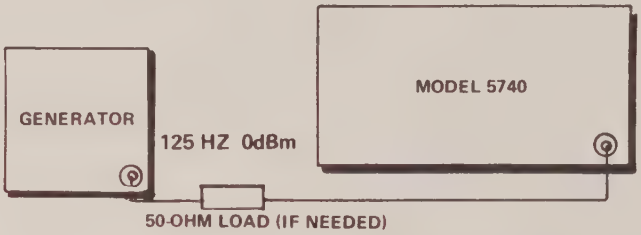
Output 0dBm into 50Ω load

Frequency: 125Hz

4.8.2 Procedure

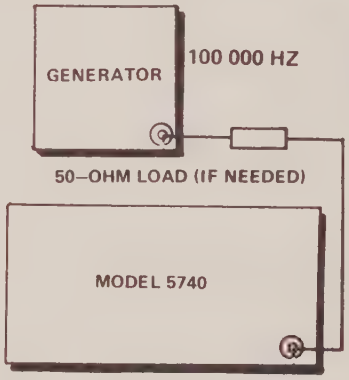
Vary the signal generator output frequency as shown in the table on Figure 4-6, and verify display values in table. If an incorrect reading is displayed, complete the test procedures of Paragraph 4.11 as an aid to trouble-shooting the Input Signal Conditioning circuit.

COPYRIGHT 1975 DATA PRECISION CORPORATION. PRINTED IN THE U.S.A.



PERIODS AVGD	PERIOD (μsec) DISPLAY	TROUBLE-SHOOTING COMMENTS
1000	8000.000 ±1	Checks Input Conditioning Ckt
100	08000.00 ±1	Checks Decimal Point
10	008000.0 ±1	&
1	0008000 ±2	Programmable Divider

Fig. 4-5. Input Signal Conditioning & Decimal Point Test Sequence



SIG GEN OUTPUT LEVEL	MODEL 5740 ATTEN	TRIGGER	FREQ DISPLAY	TROUBLE-SHOOTING COMMENTS
0 dBm	x1	Center	00100.00 ±1	
-27 dBm	x1	Adjust	00100.00±1	
-27 dBm	x20	Adjust	0 or Miscount	Checks ATTEN
0 dBm	x1	Full CW	0 or Miscount	
8 dBm	x1	Full CW	00100.00 ±1	Checks plus(+) TRIGGER
0 dBm	x1	Full CCW	0 or Miscount	
8 dBm	x1	Full CCW	00100.00 ±1	Checks minus(–) TRIGGER

4.9 PROGRAMMABLE DIVIDER AND DECIMAL POINT CONTROL CHECK (FIG. 4-7)

4.9.1 Set-UP

Model 5740

Mode Switch (S4): SEC/FREQ

Rotary Switch (S3): See Figure 4-7

Signal Generator

See Figure 4-7

4.9.2 Procedure

Position Rotary Switch (S3) and vary the Signal Generator output as shown for each step in Figure 4-7. Verify output reading according to value in table of Figure 4-7. Observe output at TP5 with oscilloscope to isolate malfunction to programmable divider or COUNTER -·-·- DISPLAY chain.

4.10 INTERCYCLE OSCILLALTOR AND CONTROL CHECK

4.10.1 Set-Up

Model 5740

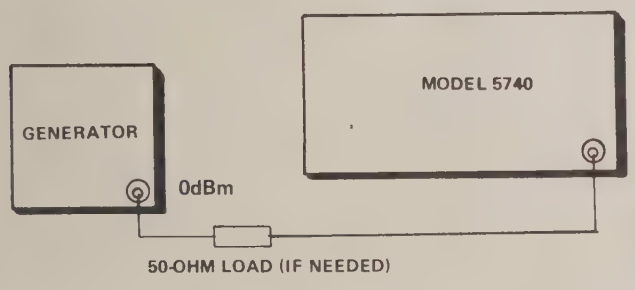
Mode Switch (S4): SEC/FREQ

Rotary Switch (S3): 100msec GATE TIME

4.10.2 Procedure

Follow procedure outlined in Figure 4-8 to trace waveform generation through to signals at TP1 and TP2. Refer to Chapter 3 and reference schematic drawing.

COPYRIGHT 1975 DATA PRECISION CORPORATION PRINTED IN THE U.S.A.



SIG GEN FREQ (HZ)	MODEL 5740 GATE TIME	MODEL 5740 DISPLAY *
1,111,111	.01 sec	001111.1 ±1
2,222,222	.1 sec	02222.22 ±1
4,444,444	1 sec	4444.444 ±1
555,555	10 sec	555.5550 ±1

*Also checks performance of Counter Chain for different digits.

Fig. 4-7. Programmable Divider Test Sequence

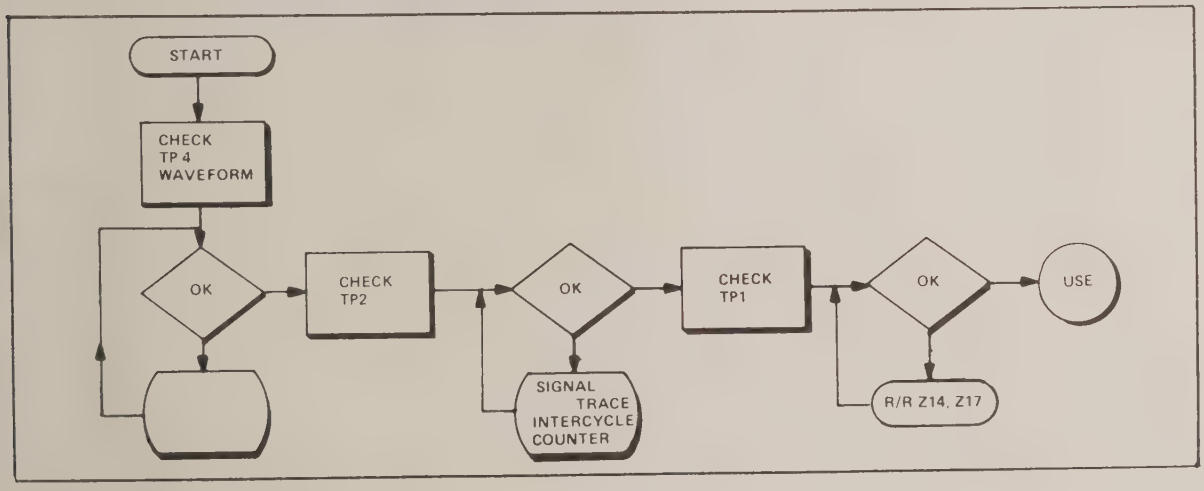


Figure 4-8. Intercycle Control Test Sequence

4.11 INPUT, SENSITIVITY, ATTEN, AND TRIGGER LEVEL CHECK (FIG. 4-6)

4.11.1 Set-Up

Model 5740

MODE Switch (S4): SEC/FREQ

Rotary Switch (S3): 100msec GATE TIME

Signal Generator

Frequency: 100000Hz

Output Level: (per procedure)

4.11.2 Procedure

Vary Model 5740 ATTEN and TRIGGER Level Controls and Signal Generator output level as shown in Figure 4-9. Verify display values against Figure 4-9 table. Signal-trace input circuit if in error.

COPYRIGHT 1975 DATA PRECISION CORPORATION. PRINTED IN THE U.S.A.

NOTES

COPYRIGHT 1975 DATA PRECISION CORPORATION PRINTED IN THE U.S.A.

5

PARTS LISTS

COPYRIGHT 1975 DATA PRECISION CORPORATION. PRINTED IN THE U.S.A.

5.1 DISPLAY ASSEMBLY

REF SYMBOL	DESCRIPTION	PART NO.
CR101	Diode, 1N4004	24-104004
DS101-DS107	Display	25-227751
Q101-103 105,107,109	Transistor 2N3904	24-233904
Q104,106 108,110	Transistor 2N5819	24-245819
R101-105	Resistor, 150 ,5%,1/4W,CC	22-021519
R106-109	Resistor, 2K,5%, 1/4W, CC	22-022029
R110,111	Resistor, 100 , 5%, 1/4W, CC	22-021019
R112-115	Resistor, 1K , 5%, 1/4W, CC	22-021029
RN101,102	Resistor Network	22-78-1007
Z101,102	IC DM7447A	24-A07447

5.2 MAIN ASSEMBLY

REF SYMBOL	DESCRIPTION	PART NO.
C1	Capacitor , 0.047uF,600V	23-212001
C2	Capacitor, 270pF,1kV, Disc	23-110036
C5	Capacitor , 10pF,1KV, Disc	23-110003
C4	Capacitor, 180pF,1KV, Disc	23-111073
C6,8,9,36,37	Capacitor, 15uF,10V	23-441003
C7	Capacitor,68uF,15V	23-442004
C10	Capacitor, 150pF	23-311015
C12	Capacitor, 2-8pF trimmer	23-310009
C13	Capacitor,0.33 uF, 10%, Mylar	23-211001
C14,15,42	Capacitor, .001uF, Disc	23-118201
C16	Capacitor, 3.3uF,10V	23-441007
C20-23,38-40,43	Capacitor, 0.01uF Disc	23-111006
C30	Capacitor, 4700uF,16V, Alum	23-610001
C31	Capacitor,1000uF,16V,Alum	23-620001
C32,33	Capacitor, 100uF,35V, Alum	23-620002
C34,35	Capacitor, 6.8uF,20V	23-441005
C41	Capacitor, .022uF,10%,50V	23-140100
CR1-4,8,203	Diode, 1N4148	24-110001
CR7	Diode, 5082-2835	24-110005
CR15,16	Diode 1N4001	24-104001
CR11	Diode Bridge	24-100020
CR17	Diode, Zener 1N963B (12V)	24-120094
CR19-22, 201,202, 300-303	Diode, 1N270	24-140270

COPYRIGHT 1975 DATA PRECISION CORPORATION PRINTED IN THE U.S.A

5.2 MAIN ASSEMBLY (Continued)

REF SYMBOL	DESCRIPTION	PART NO.
Q1	Transistor, FET (V10. DOT)	24-48-1074-03
Q2	Transistor, MPS2369	24-232369
Q3	Transistor,2N3906	24-243906
Q4	Transistor, 2N6027	24-206027
Q5	Transistor, 2N3904	24-233904
Q10,12	Transistor, 2N5818	24-235818
Q11	Transistor	24-220P32
R1	Resistor, 68K,5%,1W,CC	22-046839
R2	Resistor, 910K,5%,1/4W,CC	22-029149
R3	REsistor, 47K,5%,1/4W,CC	22-024739
R4,23,36,37, 38,39,40,16,18 R5,27,54	Resistor, 100 , 5%, 1/4W,CC	22-021019
56,61,66,14,15	Resistor, 1K,5%,1/4W,CC	22-021029
R6,7	Resistor, 1.5K,1%, RN55D	22-331501
R8,11	Resistor, 3.01K, 1%,RN55D	22-333011
R9,10	Resistor, 1.82K,1%RN60D	22-361821
R12,13	Resistor, 1.5K,5%,1/4W,CC	22-021529
R17,19	Resistor, 220 ,5%,1/4W,CC	22-022219
R20	Resistor, 620 ,5%,1/4W,CC	22-026219
R21	Resistor, 200 ,5%,1/4W,CC	22-022019
R22,48	Resistor, 470 ,5%,1/4W,CC	22-024719
R24,28,29, 30,55,62-65,201-206,300-302	Resistor,4.7K,5%,1/4W,CC	22-024729
R25,60	Resistor,3K,5%,1/4W,CC	22-023029
R26,32	Resistor,20K,5%,1/4W,CC	22-022039
R31	Resistor,300K,5%,1/4W,CC	22-023049
R33	Resistor,30K,5%,1/4W,CC	22-023039
R35	Resistor, Variable 10K	22-78-1004
R50	Resistor, 510 ,5%, 1/2W,CC	22-035119
R51	Resistor, 12.1K,1%,RN55D	22-331212
R52	Resistor Variable, 1K	22-640001
R53,58	Resistor, 4.75K,1%, RN55D	22-334751
R57	Resistor, 47 ,5%, 1/4W,CC	22-024709
R59	Resistor, 5.76K,1%, RN55D	22-335761
R67,68	Resistor, 10 ,5%, 1/4W	22-021009
Y1	Crystal,10MHz	878-1001
Z1	IC Ctr, Decoder Latch	24-L00003
Z2-4,22	IC,9946	24-469946
Z5	IC,7408	24-A07408
Z6,7,8	IC, 7475	24-A07475
Z9	IC, 74S113	24-E74S113
Z10	IC, Selected 74S113	24-E74S113-01
Z11	IC,MC10216P	24-N10216
Z12,13,23	IC,7490	24-A07490
Z14	IC,9944	24-469944
Z15	IC,74S10	24-E74S10
Z16	IC,9949	24-469949
Z17,300	IC, 9937	24-469937
Z18	IC, 7410	24-A07410
Z19	IC, MK5009P OR N	24-L05009
Z20	IC,7473	24-A07473
Z21	IC,7476	24-A07476
Z24	IC,5558V	24-405558
Z201-204	IC,93L10	24-C93L10

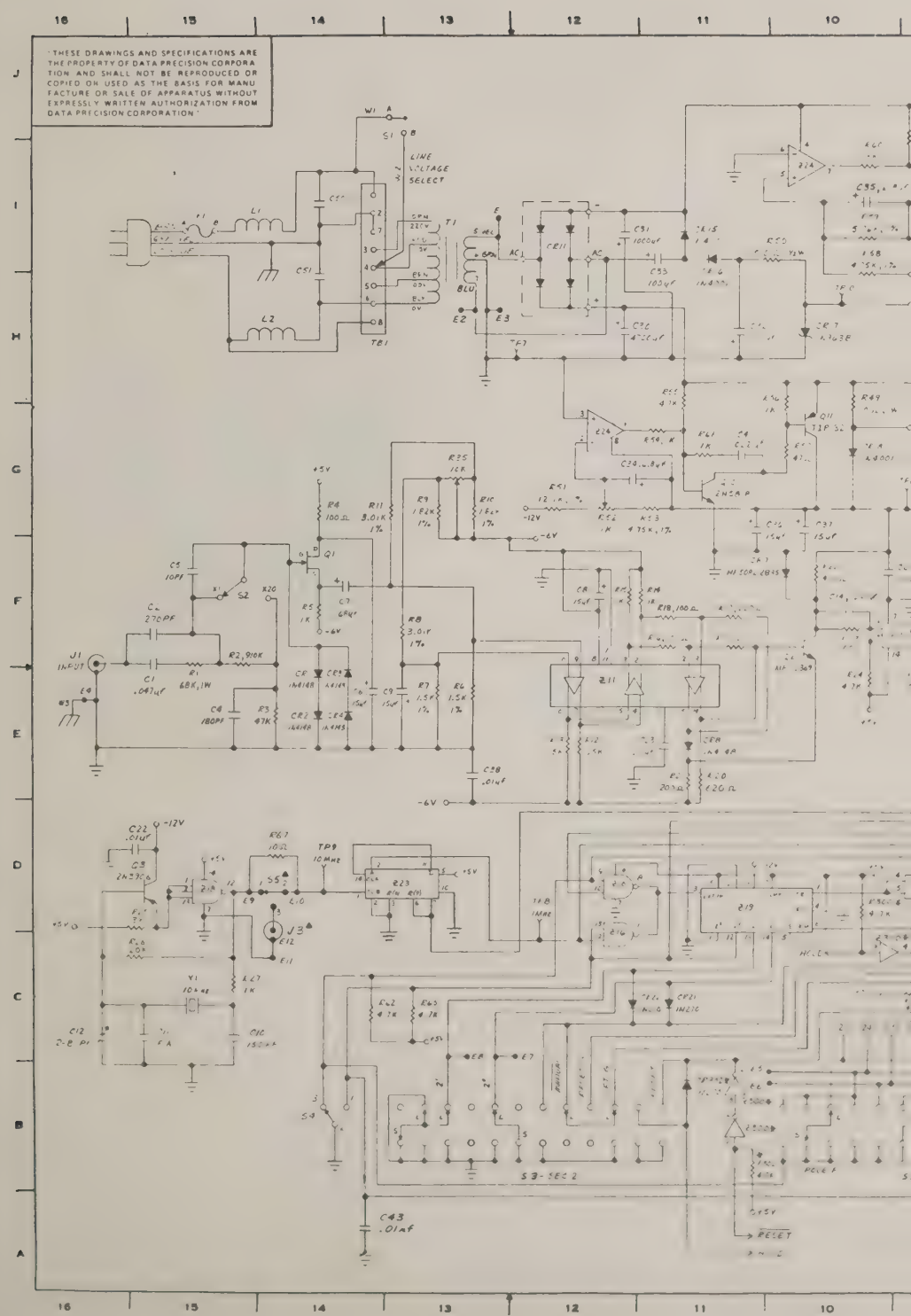
COPYRIGHT 1975 DATA PRECISION CORPORATION. PRINTED IN THE U.S.A

6

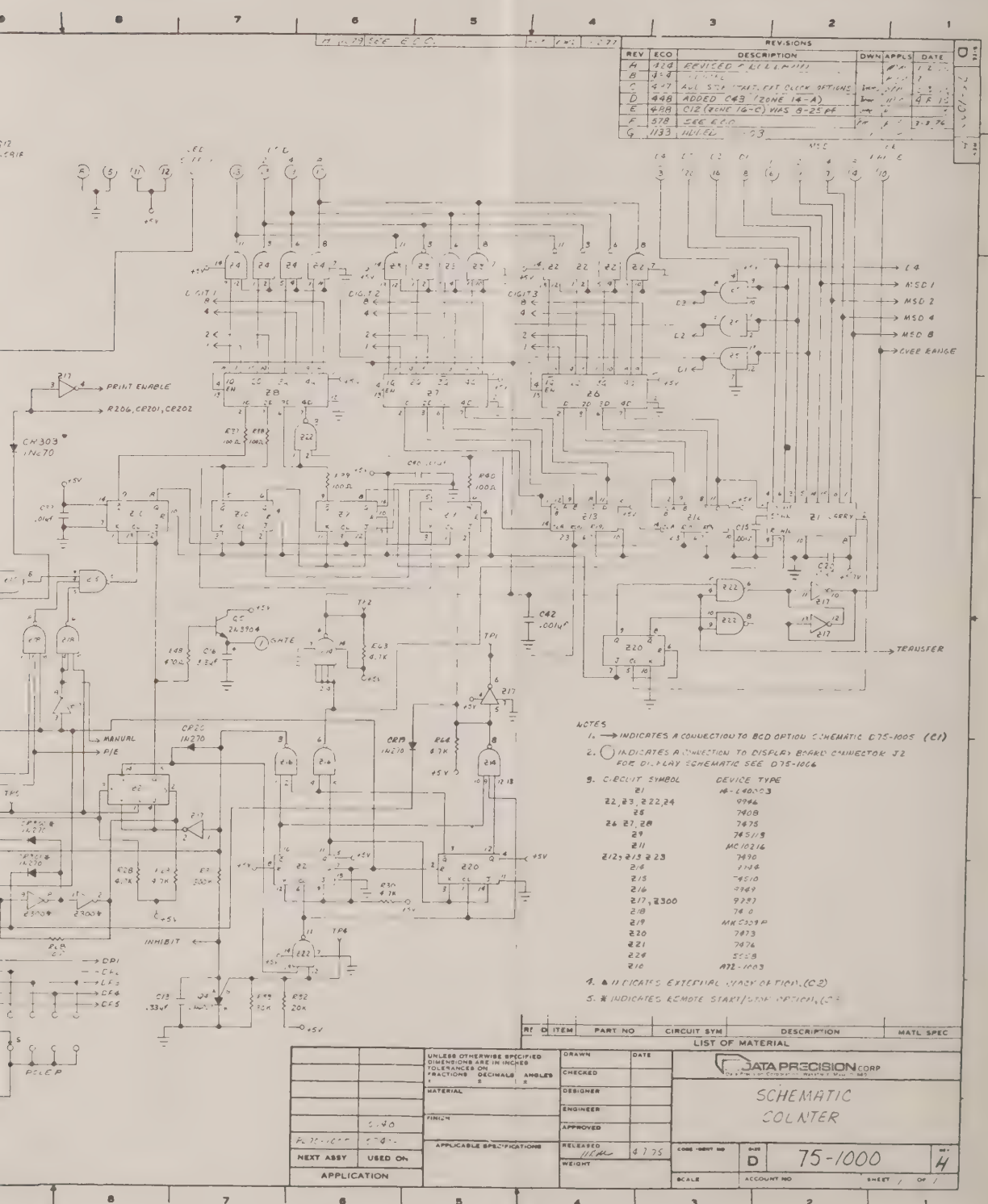
REFERENCE DRAWINGS

6.1 MAIN PC BOARD
6.2 DISPLAY
6.3 BCD OPTION

COPYRIGHT 1975 DATA PRECISION CORPORATION. PRINTED IN THE U.S.A.

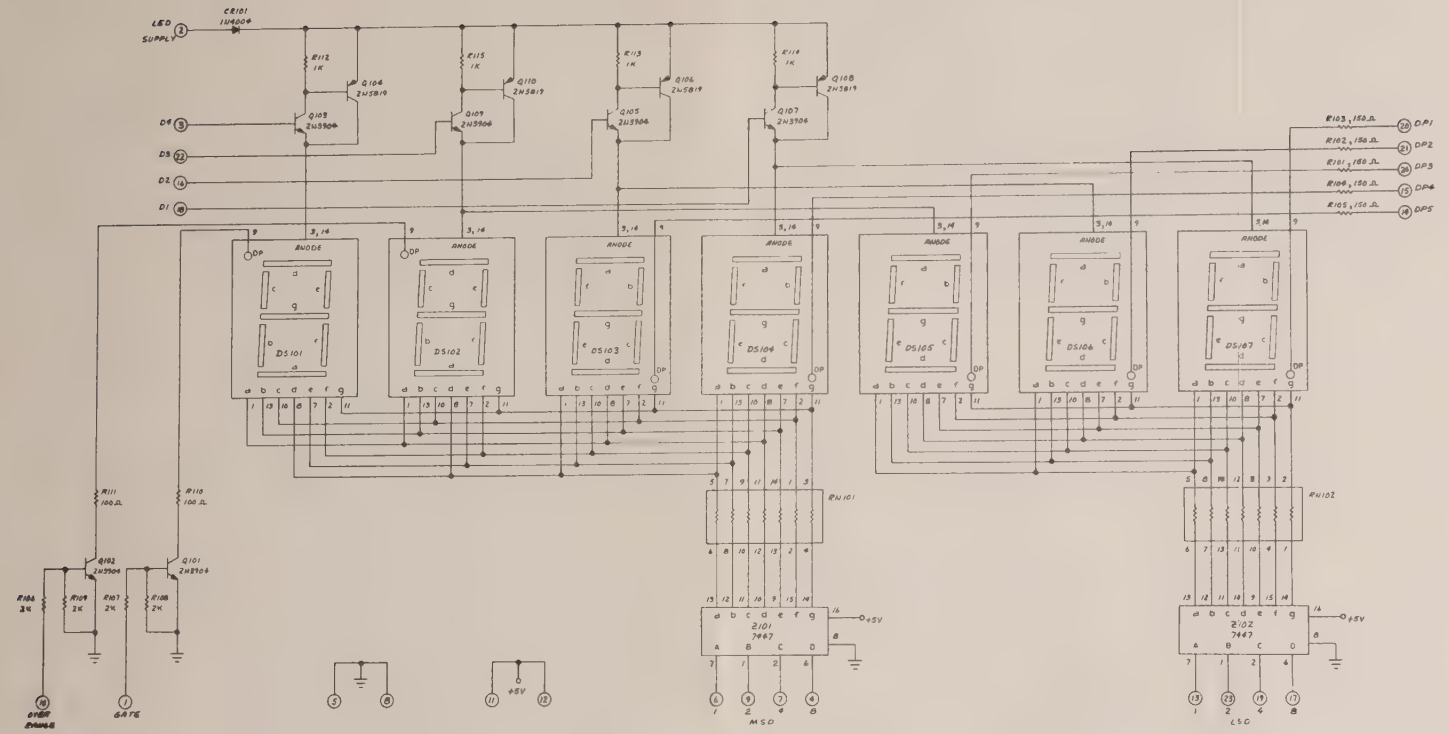

THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF DATA PRECISION CORPORATION AND SHALL NOT BE REPRODUCED OR COPIED OR USED AS THE BASIS FOR MANUFACTURE OR SALE OF APPARATUS WITHOUT EXPRESSLY WRITTEN AUTHORIZATION FROM DATA PRECISION CORPORATION.
LINE VOLTAGE SELECT
INPUT
+5V
-12V
-6V
10MHz
S3-SEC 2
RELET

COPYRIGHT 1975 DATA PRECISION CORPORATION PRINTED IN THE U.S.A.


REVISIONS
REV | ECO | DESCRIPTION | DWN | APPD | DATE
A 414 REVISED PER ECO
B 438
C 447 ADD START, EXT CLOCK OPTIONS
D 448 ADDED C43 (ZONE 14-A)
E 488 C12 (ZONE 16-C) WAS 8-25 pF
F 578 SEE ECO
G 1133 INITIAL
LSD
MSD 1
MSD 2
MSD 4
MSD 8
OVER RANGE
PRINT ENABLE
R206, CR201, CR202
GATE
MANUAL
P/E
INHIBIT
TRANSFER
NOTES
1. → INDICATES A CONNECTION TO BCD OPTION SCHEMATIC D75-1005 (C1)
2. ○ INDICATES A CONNECTION TO DISPLAY BOARD CONNECTOR J2 FOR DISPLAY SCHEMATIC SEE D75-1064
3. CIRCUIT SYMBOL / DEVICE TYPE
21 MC-L40003
22,23,222,24 9946
25 7408
26 27,28 7475
29 7451/9
211 MC10216
212,213,223 7490
214 7438
215 74510
216 9969
217, 2300 9097
218 74 0
219 MK5309P
220 7873
221 7476
224 5559
210 A72-1003
4. ▲ INDICATES EXTERNAL MARK OPTION. (C2)
5. * INDICATES REMOTE START/STOP OPTION. (C
ITEM | PART NO | CIRCUIT SYM | DESCRIPTION | MATL SPEC
LIST OF MATERIAL
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS
DRAWN
CHECKED
DESIGNER
ENGINEER
APPROVED
RELEASED
WEIGHT
DATE
NEXT ASSY USED ON
APPLICATION
DATA PRECISION CORP
SCHEMATIC
COUNTER
SIZE D
75-1000
REV 4
SCALE
ACCOUNT NO
SHEET 1 OF 1

REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPR	DATE
A	824	REVISED & REDRAWN			11-76

D | 75-1006 | A



NOTES
1. ○ INDICATES A CONNECTION TO THE DISPLAY CARD CONNECTOR, J2. FOR MAIN CARD SCHEMATIC SEE D75-1000.

REQD	ITEM	PART NO	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
FRACTIONS DECIMALS ANGLES
X
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS

DRAWN | DATE
CHECKED
DESIGNER
ENGINEER
APPROVED
RELEASED
WEIGHT

DATA PRECISION CORP

SCHEMATIC
COUNTER
H.P. DISPLAY CARD

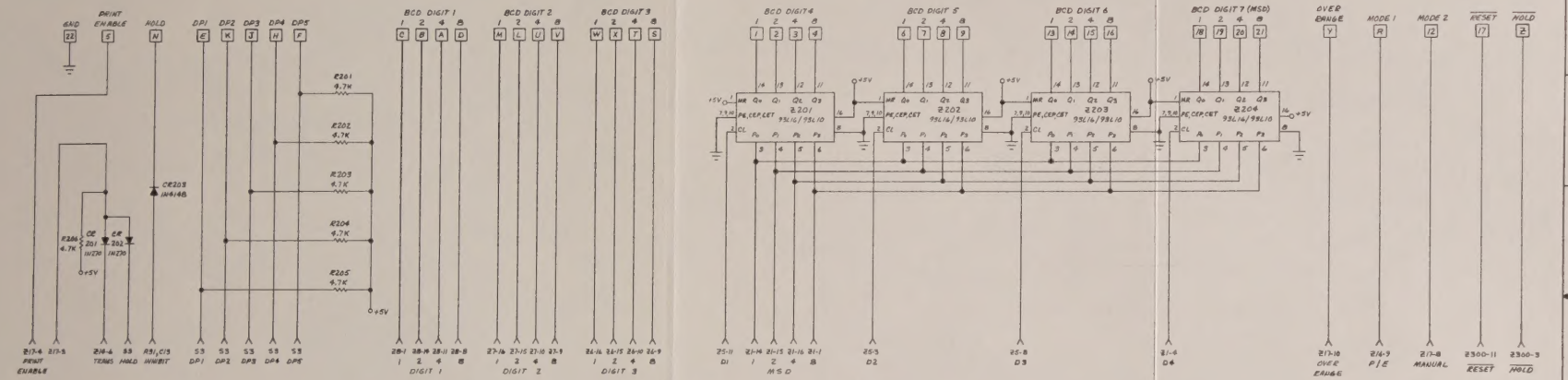
P.70-1006	5740-1	D	75-1006 A
NEXT ASSY	USED ON	SCALE	SHEET 1 OF 1
APPLICATION			

COPYRIGHT 1975 DATA PRECISION CORPORATION PRINTED IN THE U.S.A.

"THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF DATA PRECISION CORPORATION AND SHALL NOT BE REPRODUCED OR COPIED OR USED AS THE BASIS FOR MANUFACTURE OR SALE OF APPARATUS WITHOUT EXPRESSLY WRITTEN AUTHORIZATION FROM DATA PRECISION CORPORATION."

REVISIONS					
REV.	ECO	DESCRIPTION	DWN	APPR.	DATE
A	437	ADDED PINOUTS TO [17] & [18]	JPC	[illegible]	5-3-75

D 75-1005 A



NOTES:
1. ⟩— INDICATES A CONNECTION FROM COUNTER SCHEMATIC D75-1000.
2. □ INDICATES A CONNECTION TO THE BCD OPTION, PC. CARD EDGE CONNECTOR.
3.

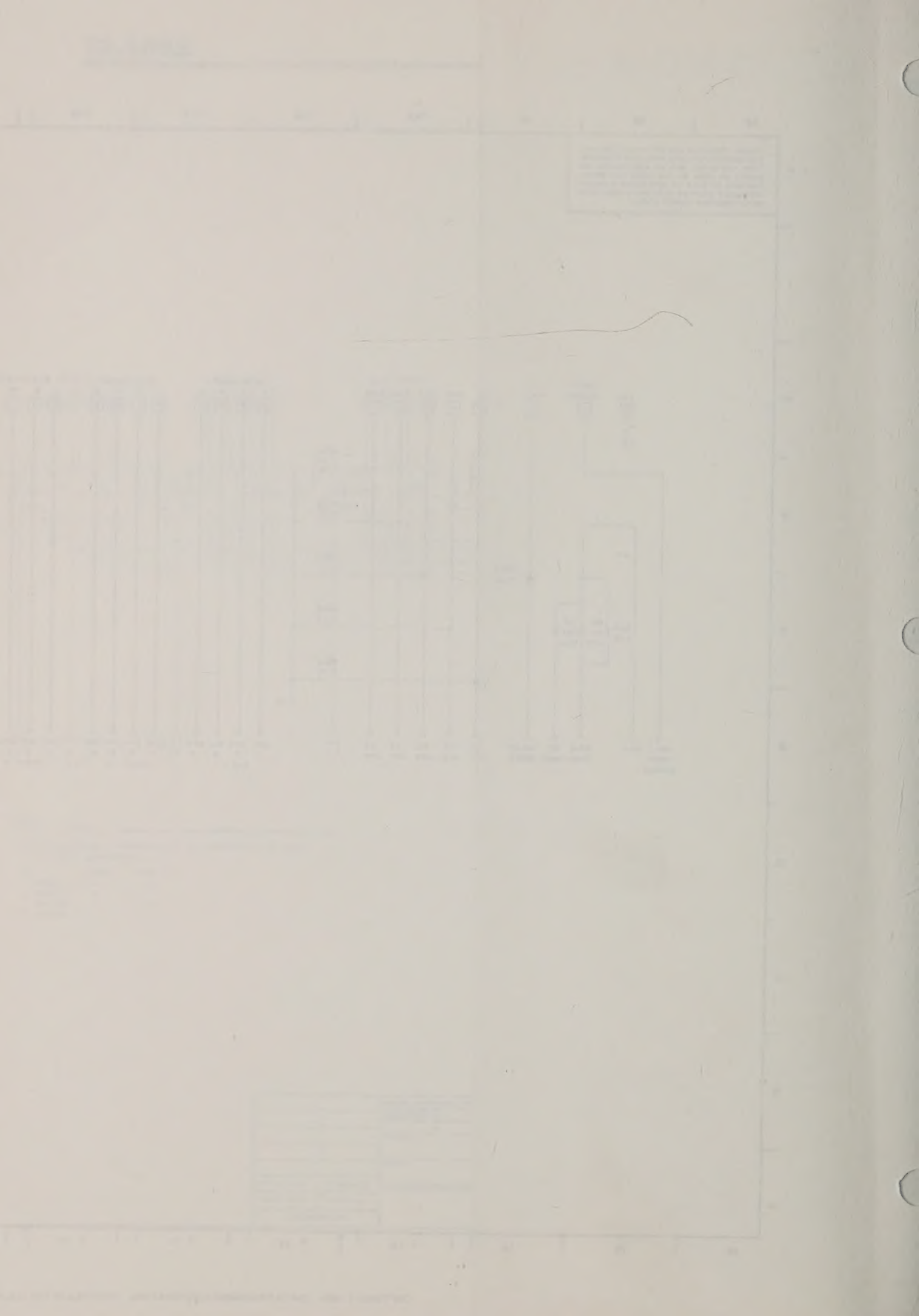
	MODE 1	MODE 2
FREQ	0	0
SEC	0	1
PER AVG	1	0
EVENTS	1	1

REQD	ITEM	PART NO.	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS ± DECIMALS ± ANGLES ±	DRAWN	DATE	DATA PRECISION CORP. Data Precision Corporation, Wakefield, Mass. 01880
		MATERIAL	CHECKED		SCHEMATIC COUNTER BCD OPTION, C1
		FINISH	DESIGNER		
P/N 70-1005	5740-C1	APPLICABLE SPECIFICATIONS	ENGINEER		
NEXT ASSY	USED ON		APPROVED		
APPLICATION			RELEASED		DWG. NO. 75-1005 SIZE D REV A
			WEIGHT		SCALE ACCOUNT NO. SHEET 1 OF 1

COPYRIGHT 1975 DATA PRECISION CORPORATION PRINTED IN THE U.S.A.



www.manualsplus.com
1012119